THE DATASHEET OF

PCM1808PWR

www.win-source.net 0086-755-83957316

PCM1808 Single-Ended, Analog-Input 24-Bit, 96-kHz Stereo ADC

1 Features

- 24-Bit Delta-Sigma Stereo A/D Converter (ADC)
- Single-Ended Voltage Input: 3 Vp-p
- High Performance:
  - THD+N: –93 dB (Typical)
  - SNR: 99 dB (Typical)
  - Dynamic Range: 99 dB (Typical)
- Oversampling Decimation Filter:
  - Oversampling Frequency: ×64
  - Pass-Band Ripple: ±0.05 dB
  - Stop-Band Attenuation: –65 dB
  - On-Chip High-Pass Filter: 0.91 Hz (48 kHz)
- Flexible PCM Audio Interface
  - Master- or Slave-Mode Selectable
  - Data Formats: 24-Bit I^2S, 24-Bit Left-Justified
- Power Down and Reset by Halting System Clock
- Analog Antialias LPF Included
- Sampling Rate: 8 kHz–96 kHz
- System Clock: 256 f_S, 384 f_S, 512 f_S
- Resolution: 24 Bits
- Dual Power Supplies:
  - 5-V for Analog
  - 3.3-V for Digital
- Package: 14-Pin TSSOP

2 Applications

- DVD Recorder
- Digital TV
- AV Amplifier or Receiver
- MD Player
- CD Recorder
- Multitrack Receiver
- Electric Musical Instrument

3 Description

The PCM1808 device is a high-performance, low-cost, single-chip, stereo analog-to-digital converter with single-ended analog voltage input. The PCM1808 device uses a delta-sigma modulator with 64-times oversampling and includes a digital decimation filter and high-pass filter that removes the dc component of the input signal. For various applications, the PCM1808 device supports master and slave mode and two data formats in serial audio interface.

The PCM1808 device supports the power-down and reset functions by means of halting the system clock.

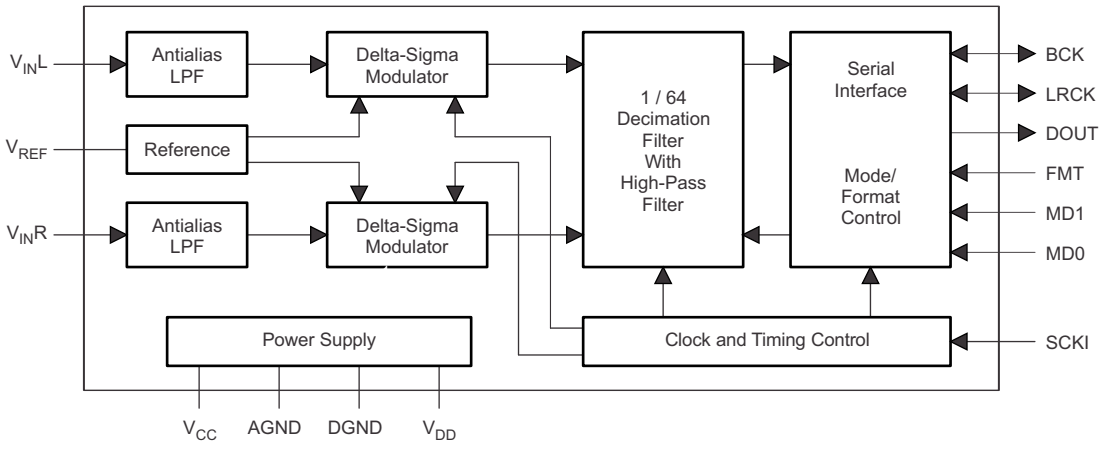
The PCM1808 device is suitable for wide variety of cost-sensitive consumer applications requiring good performance and operation with a 5-V analog supply and 3.3-V digital supply. Fabrication of the PCM1808 device uses a highly advanced CMOS process. The device is available in a small, 14-pin TSSOP package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
PCM1808	TSSOP (14)	4.40 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

PCM1808 Block Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Revision A (August 2006) to Revision B **Page**

- Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section. ... 1

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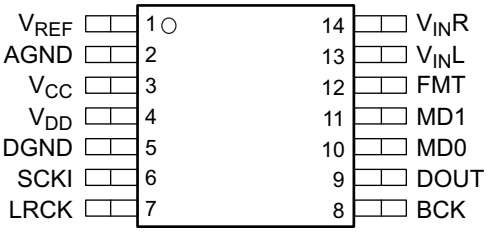
5 Pin Configuration and Functions

14-Pin TSSOP
PW Package
Top View



P0032-02

Pin Functions

PIN		I/O	DESCRIPTION
NAME	PIN		
AGND	2	—	Analog GND
BCK	8	I/O	Audio-data bit-clock input or output (1)
DGND	5	—	Digital GND
DOUT	9	O	Audio-data digital output
FMT	12	I	Audio-interface format select (2)
LRCK	7	I/O	Audio-data latch-enable input or output (1)
MD0	10	I	Audio-interface mode select 0 (2)
MD1	11	I	Audio-interface mode select 1 (2)
SCKI	6	I	System clock input; 256 f_S, 384 f_S or 512 f_S (3)
V_{CC}	3	—	Analog power supply, 5-V
V_{DD}	4	—	Digital power supply, 3.3-V
$V_{IN}L$	13	I	Analog input, L-channel
$V_{IN}R$	14	I	Analog input, R-channel
V_{REF}	1	—	Reference-voltage decoupling (= 0.5 V_{CC})

(1) Schmitt-trigger input with internal pulldown (50-kΩ, typical)
(2) Schmitt-trigger input with internal pulldown (50-kΩ, typical), 5-V tolerant
(3) Schmitt-trigger input, 5-V tolerant

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6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CC}	Analog supply voltage		–0.3	6.5	V
V_{DD}	Digital supply voltage		–0.3	4	V
	Ground voltage differences	AGND, DGND		±0.1	V
	Digital input voltage	LRCK, BCK, DOUT	–0.3	(V_{DD} + 0.3 V) < 4	V
		SCKI, MD0, MD1, FMT	–0.3	6.5	V
$V_{IN}L$, $V_{IN}R$, V_{REF}	Analog input voltage		–0.3	(V_{CC} + 0.3 V) < 6.5	V
	Input current (any pins except supplies)			±10	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±4000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Analog supply voltage (see *Power Supply Recommendations*)		4.5	5	5.5	V
V_{DD}	Digital supply voltage		2.7	3.3	3.6	V
	Analog input voltage, full scale (–0 dB)	V_{CC} = 5 V			3	Vp-p
V_{IH} (1)	High input logic level		2		V_{DD}	VDC
V_{IL} (1)	Low input logic level		0		0.8	VDC
V_{IH} (2) (3)	High input logic level		2		5.5	VDC
V_{IL} (2) (3)	Low input logic level		0		0.8	VDC
	Digital input logic family		TTL compatible			
	Digital input clock frequency, system clock		2.048		49.152	MHz
	Digital input clock frequency, sampling clock		8		96	kHz
	Digital output load capacitance				20	pF
T_A	Operating ambient temperature range		–40		85	°C
T_J	Junction temperature				150	°C

(1) Pins 7, 8: LRCK, BCK (Schmitt-trigger input, with 50-kΩ typical pulldown resistor, in slave mode)
(2) Pin 6: SCKI (Schmitt-trigger input, 5-V tolerant)
(3) Pins 10–12: MD0, MD1, FMT (Schmitt-trigger input, with 50-kΩ typical pulldown resistor, 5-V tolerant)

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6.4 Thermal Information

THERMAL METRIC(1)		PCM1808 PW (TSSOP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	89.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	25.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	30.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	29.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

All specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, master mode, f_S = 48 kHz, system clock = 512 f_S, 24-bit data, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution			24		Bits
DATA FORMAT						
	Audio data interface format			I^2S, left-justified		
	Audio data bit length			24		Bits
	Audio data format			MSB-first, 2s complement		
f_S	Sampling frequency		8	48	96	kHz
	System clock frequency	256 f_S	2.048	12.288	24.576	MHz
		384 f_S	3.072	18.432	36.864	
		512 f_S	4.096	24.576	49.152	
INPUT LOGIC						
V_{IH} (1)	High input logic level		2		V_{DD}	VDC
V_{IL} (1)	Low input logic level		0		0.8	VDC
V_{IH} (2) (3)	High input logic level		2		5.5	VDC
V_{IL} (2) (3)	Low input logic level		0		0.8	VDC
I_{IH} (2)	High input logic current	$V_{IN} = V_{DD}$			±10	µA
I_{IL} (2)	Low input logic current	V_{IN} = 0 V			±10	µA
I_{IH} (1) (3)	High input logic current	$V_{IN} = V_{DD}$		65	100	µA
I_{IL} (1) (3)	Low input logic current	V_{IN} = 0 V			±10	µA
OUTPUT LOGIC						
V_{OH} (4)	High output logic level	I_{OUT} = –4 mA	2.8			VDC
V_{OL} (4)	Low output logic level	I_{OUT} = 4 mA			0.5	VDC
DC ACCURACY						
	Gain mismatch, channel-to-channel			±1	±3	% of FSR
	Gain error			±3	±6	% of FSR

(1) Pins 7, 8: LRCK, BCK (Schmitt-trigger input, with 50-kΩ typical pulldown resistor, in slave mode)
(2) Pin 6: SCKI (Schmitt-trigger input, 5-V tolerant)
(3) Pins 10–12: MD0, MD1, FMT (Schmitt-trigger input, with 50-kΩ typical pulldown resistor, 5-V tolerant)
(4) Pins 7–9: LRCK, BCK (in master mode), DOUT

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Electrical Characteristics (continued)

All specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, master mode, f_S = 48 kHz, system clock = 512 f_S, 24-bit data, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE (5)						
THD+N	Total harmonic distortion + noise	V_{IN} = –0.5 dB, f_S = 48 kHz		–93	–87	dB
		V_{IN} = –0.5 dB, f_S = 96 kHz (6)		–87		
		V_{IN} = –60 dB, f_S = 48 kHz		–37		
		V_{IN} = –60 dB, f_S = 96 kHz (6)		–39		
	Dynamic range	f_S = 48 kHz, A-weighted	95	99		dBVDC
		f_S = 96 kHz, A-weighted (6)		101		
S/N	Signal-to-noise ratio	f_S = 48 kHz, A-weighted	95	99		dB
		f_S = 96 kHz, A-weighted (6)		101		
	Channel separation	f_S = 48 kHz	93	97		dB
		f_S = 96 kHz (6)		91		
ANALOG INPUT						
	Input voltage			0.6 V_{CC}		Vp-p
	Center voltage (V_{REF})			0.5 V_{CC}		V
	Input impedance			60		kΩ
	Antialiasing filter frequency response	–3 dB		1.3		MHz
DIGITAL FILTER PERFORMANCE						
	Pass band				0.454 f_S	Hz
	Stop band		0.583 f_S			Hz
	Pass-band ripple				±0.05	dB
	Stop-band attenuation		–65			dB
	Delay time			17.4 / f_S		
	HPF frequency response	–3 dB		0.019 f_S / 1000		
POWER SUPPLY REQUIREMENTS						
I_{CC}	Analog supply current (7)	f_S = 48 kHz, 96 kHz (6)		8.6	11	mA
		Powered down (8)		1		µA
I_{DD}	Digital supply current (7)	f_S = 48 kHz		5.9	8	mA
		f_S = 96 kHz (6)		10.2		mA
		Powered down (8)		150		µA
	Power dissipation (7)	f_S = 48 kHz		62	81	mW
		f_S = 96 kHz (6)		77		
		Powered down (8)		500		µW

(5) Testing of analog performance specifications uses an audio measurement system by Audio Precision™ with 400-Hz HPF and 20-kHz LPF in RMS mode.
(6) f_S = 96 kHz, system clock = 256 f_S.
(7) Minimum load on LRCK (pin 7), BCK (pin 8), DOUT (pin 9)
(8) Power-down and reset functions enabled by halting SCKI, BCK, LRCK.

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6.6 Timing Requirements

		MIN	NOM	MAX	UNIT
SYSTEM CLOCK TIMING					
$t_{w(SCKH)}$	System clock pulse duration, HIGH	8			ns
$t_{w(SCKL)}$	System clock pulse duration, LOW	8			ns
	System clock duty cycle	40%		60%	
CLOCK-HALT POWER-DOWN AND RESET TIMING					
$t_{(CKR)}$	Delay time from SCKI halt to internal reset	4			µs
$t_{(RST)}$	Delay time from SCKI resume to reset release			1024 SCKI	µs
$t_{(REL)}$	Delay time from reset release to DOUT output			8960 / f_S	µs
AUDIO DATA INTERFACE TIMING (Slave Mode: LRCK and BCK Work as Inputs)(1)					
$t_{(BCKP)}$	BCK period	1 / (64 f_S)			ns
$t_{(BCKH)}$	BCK pulse duration, HIGH	1.5 × $t_{(SCKI)}$			ns
$t_{(BCKL)}$	BCK pulse duration, LOW	1.5 × $t_{(SCKI)}$			ns
$t_{(LRSU)}$	LRCK setup time to BCK rising edge	50			ns
$t_{(LRHD)}$	LRCK hold time to BCK rising edge	10			ns
$t_{(LRCP)}$	LRCH period	10			µs
$t_{(CKDO)}$	Delay time, BCK falling edge to DOUT valid	–10		40	ns
$t_{(LRDO)}$	Delay time, LRCK edge to DOUT valid	–10		40	ns
t_r	Rise time of all signals			20	ns
t_f	Fall time of all signals			20	ns
AUDIO DATA INTERFACE TIMING (Master Mode: LRCK and BCK Work as Outputs)(2)					
$t_{(BCKP)}$	BCK period	150	1 / (64 f_S)	2000	ns
$t_{(BCKH)}$	BCK pulse duration, HIGH	65		1200	ns
$t_{(BCKL)}$	BCK pulse duration, LOW	65		1200	ns
$t_{(CKLR)}$	Delay time, BCK falling edge to LRCK valid	–10		20	ns
$t_{(LRCP)}$	LRCK period	10	1 / f_S	125	ns
$t_{(CKDO)}$	Delay time, BCK falling edge to DOUT valid	–10		20	ns
$t_{(LRDO)}$	Delay time, LRCK edge to DOUT valid	–10		20	ns
t_r	Rise time of all signals			20	ns
t_f	Fall time of all signals			20	ns
AUDIO CLOCK INTERFACE TIMING (Master Mode: BCK Work as Outputs)(3)					
$t_{(SCKBCK)}$	Delay time, SCKI rising edge to BCK edge	5		30	ns

(1) Timing measurement reference level is 1.4 V for input and 0.5 V_{DD} for output. Rise and fall times are from 10% to 90% of the input-output signal swing. Load capacitance of DOUT is 20 pF. $t_{(SCKI)}$ is the SCKI period.
(2) Timing measurement reference level is 0.5 V_{DD}. Rise and fall times are from 10% to 90% of the input-output signal swing. Load capacitance of all signals is 20 pF.
(3) Timing measurement reference level is 1.4 V for input and 0.5 V_{DD} for output. Load capacitance of BCK is 20 pF. This timing applies when SCKI frequency is less than 25 MHz.

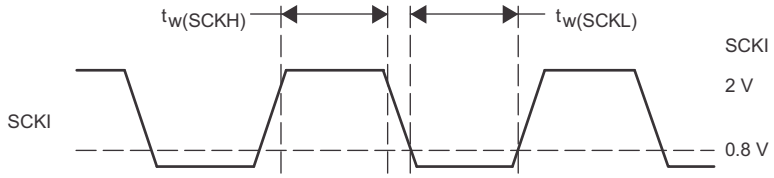

Figure 1. System Clock Timing

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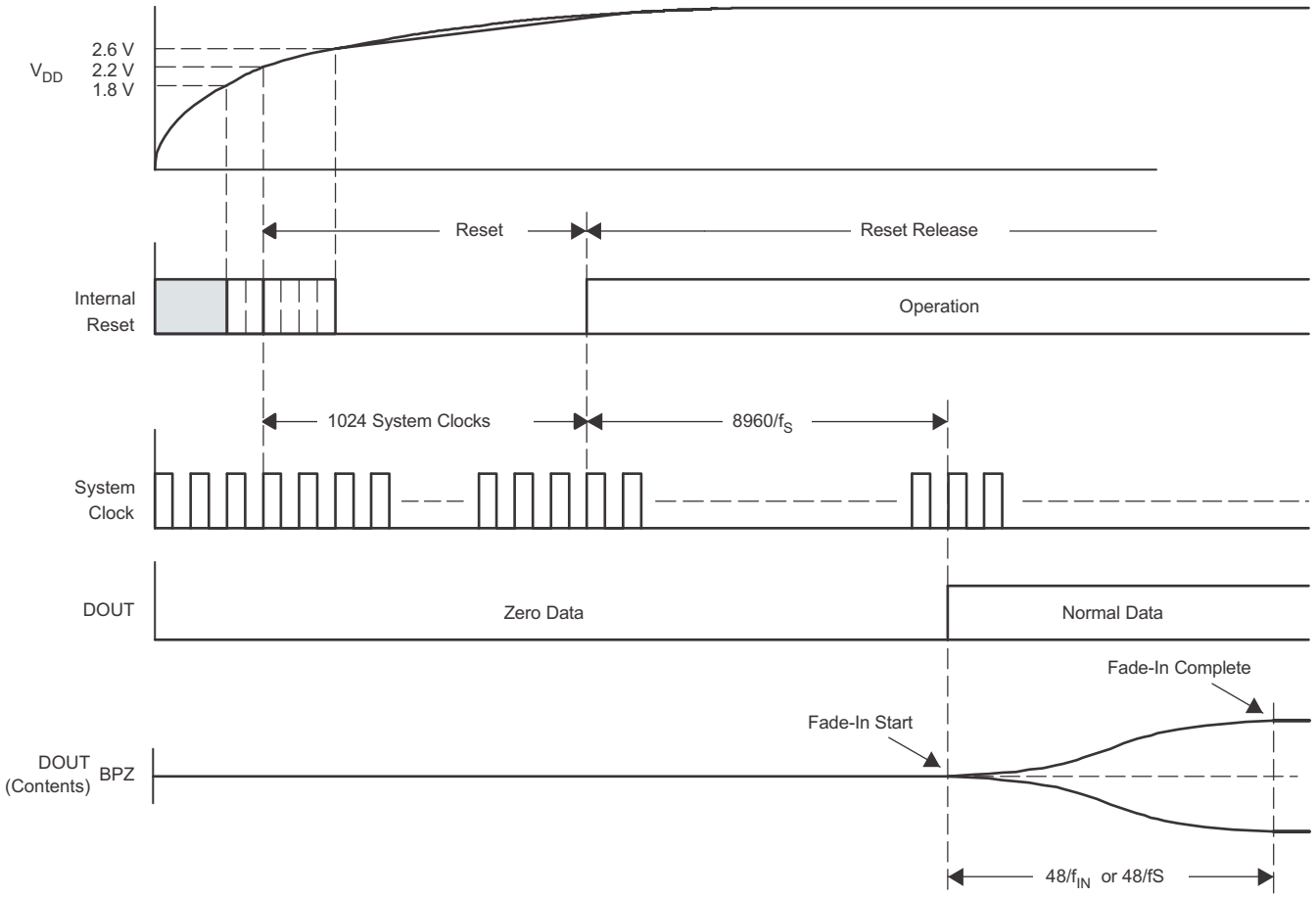

Figure 2. Power-On Timing

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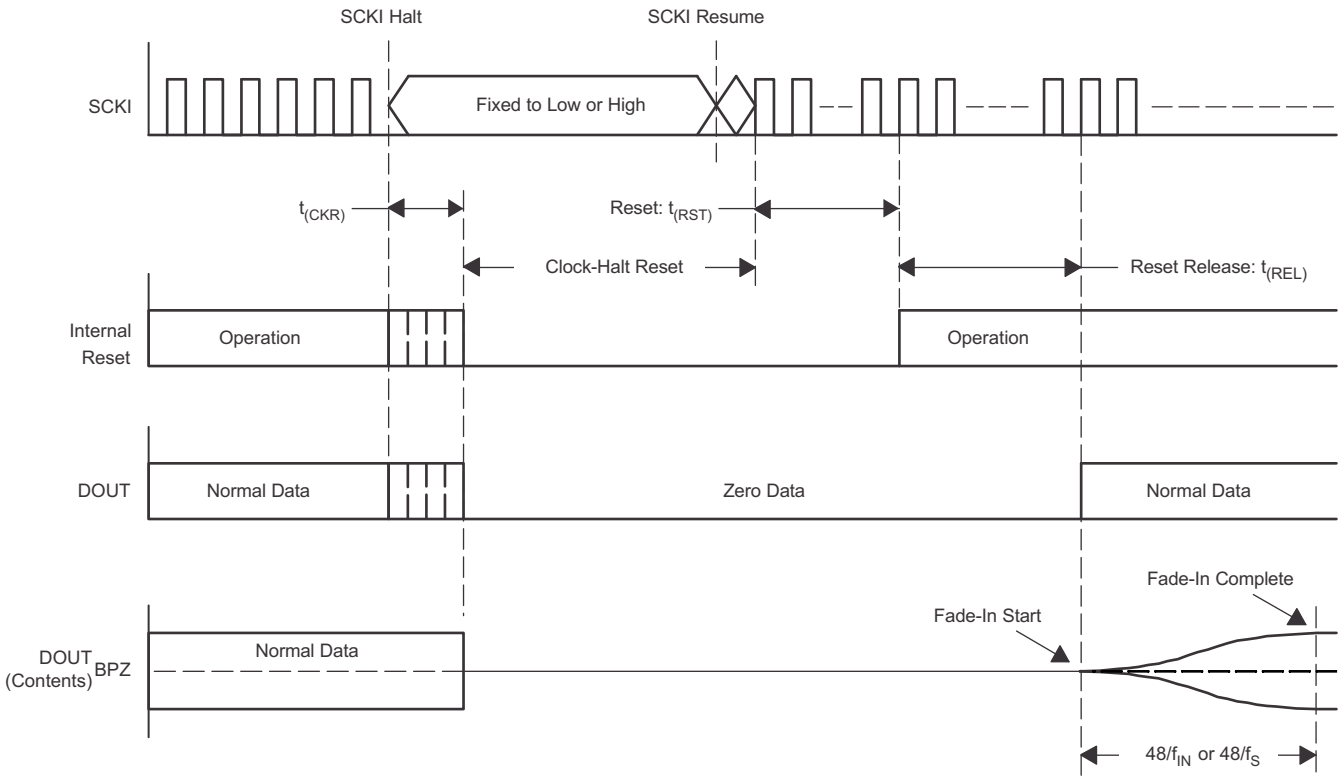

Figure 3. Clock-Halt Power-Down and Reset Timing

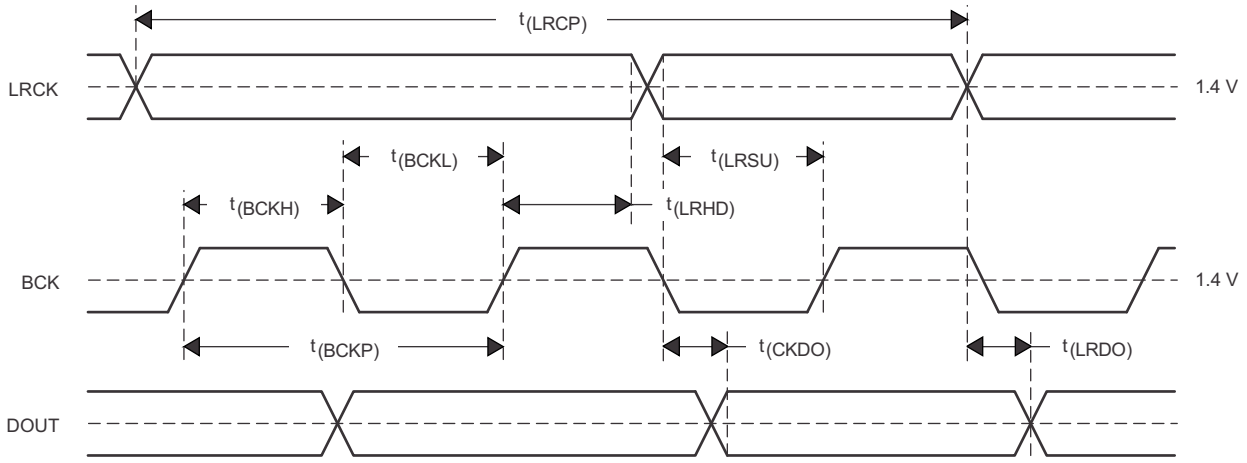

Figure 4. Audio Data Interface Timing (Slave Mode: LRCK and BCK Work as Inputs)

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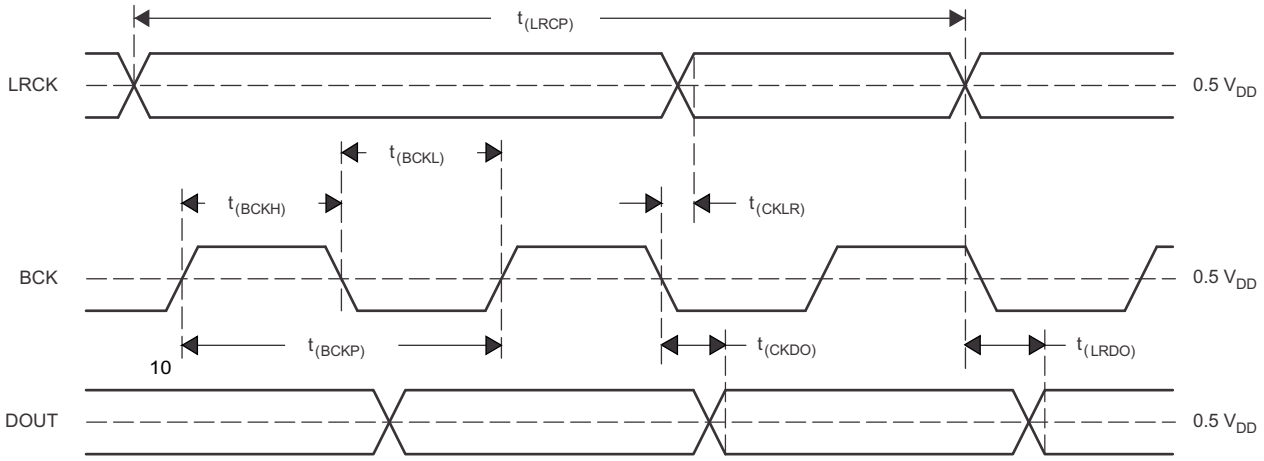

Figure 5. Audio Data Interface Timing (Master Mode: LRCK and BCK Work as Outputs)

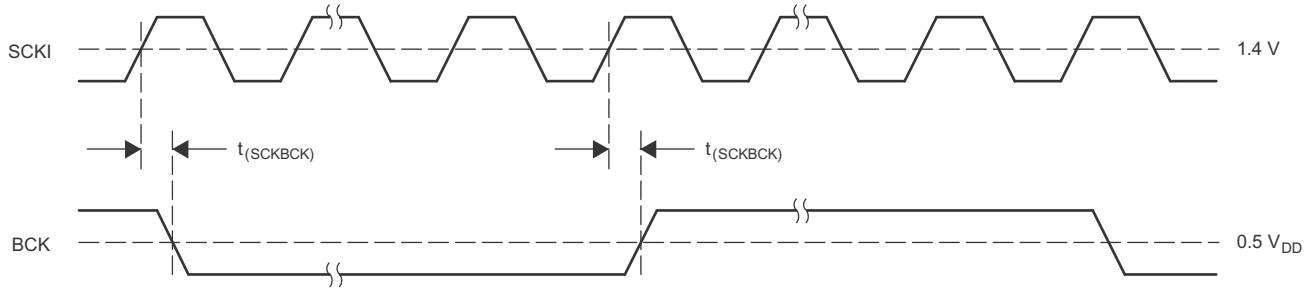

Figure 6. Audio Clock Interface Timing (Master Mode: BCK Works as Output)

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6.7 Typical Characteristics

All specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, master mode, f_S = 48 kHz, system clock = 512 f_S, 24-bit data, unless otherwise noted.

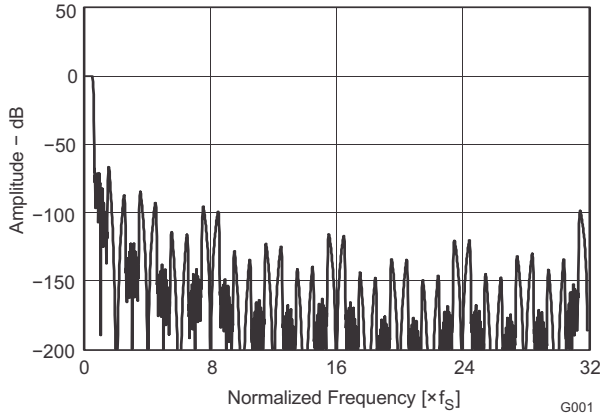

Figure 7. Decimation-Filter Frequency Response Overall Characteristics

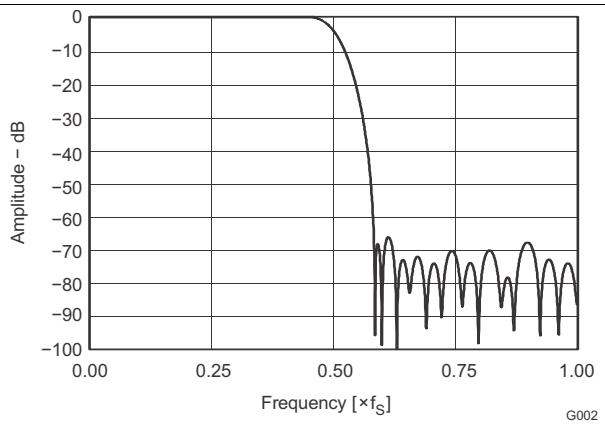

Figure 8. Decimation-Filter Frequency Response Stop-Band Attenuation Characteristics

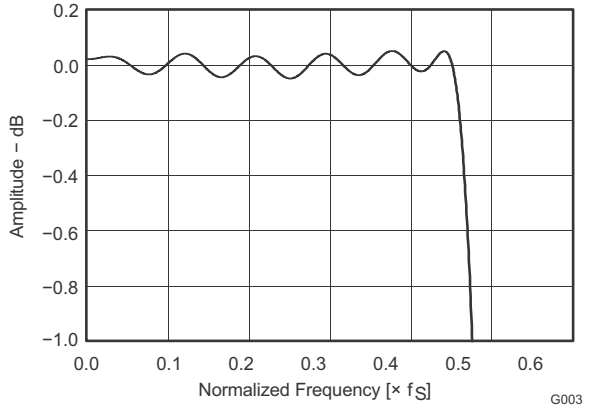

Figure 9. Decimation-Filter Frequency Response Pass-Band Ripple Characteristics

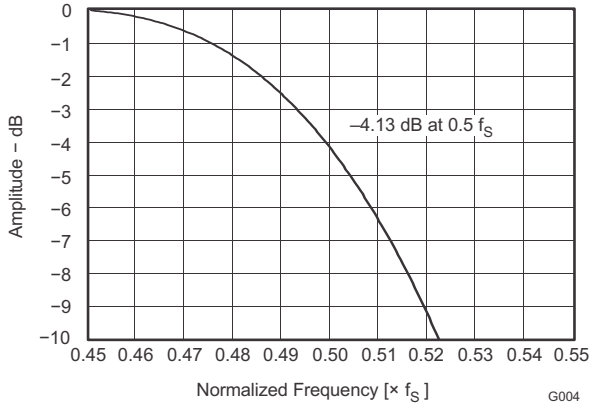

Figure 10. Decimation-Filter Frequency Response Transition-Band Characteristics

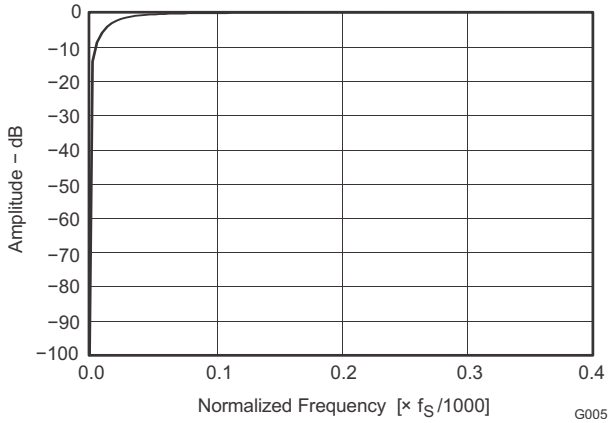

Figure 11. High-Pass Filter Frequency Response HPF Stop-Band Characteristics

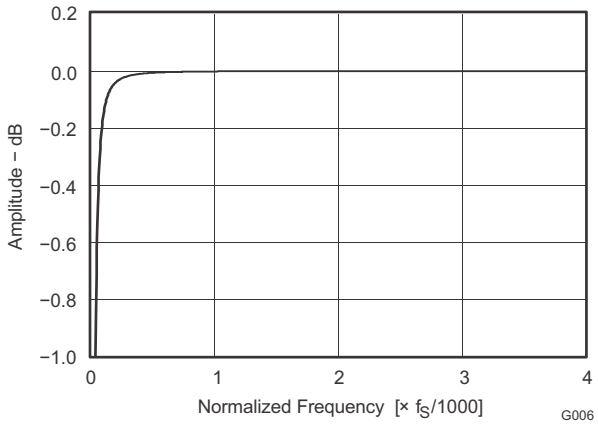

Figure 12. High-Pass Filter Frequency Response HPF Stop-Band Characteristics

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Typical Characteristics (continued)

All specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, master mode, f_S = 48 kHz, system clock = 512 f_S, 24-bit data, unless otherwise noted.

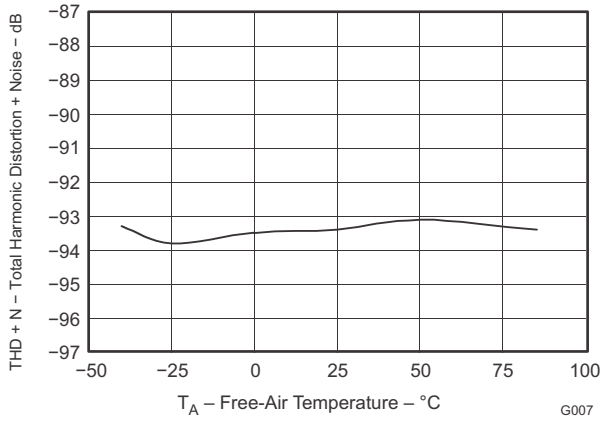

Figure 13. THD+N vs Temperature

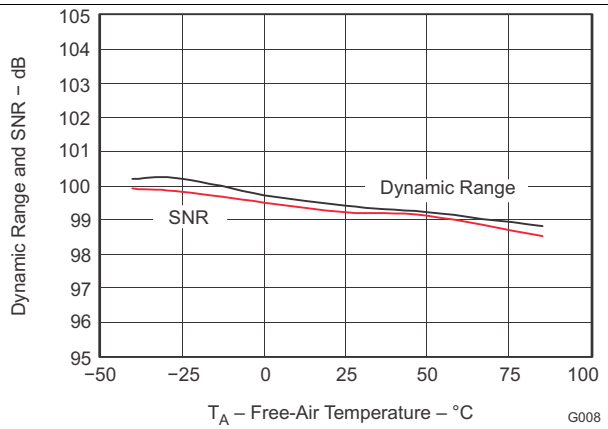

Figure 14. Dynamic Range and SNR vs Temperature

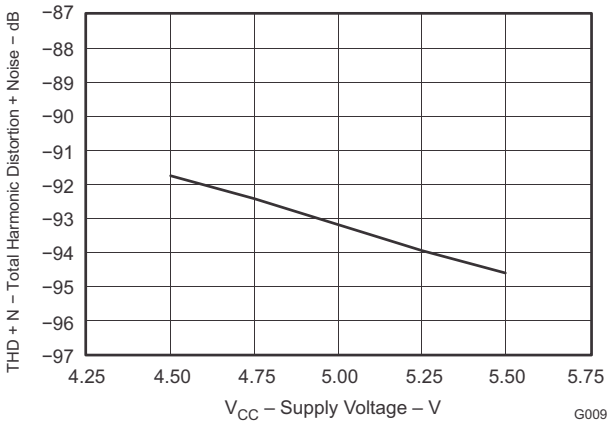

Figure 15. THD+N vs Supply Voltage

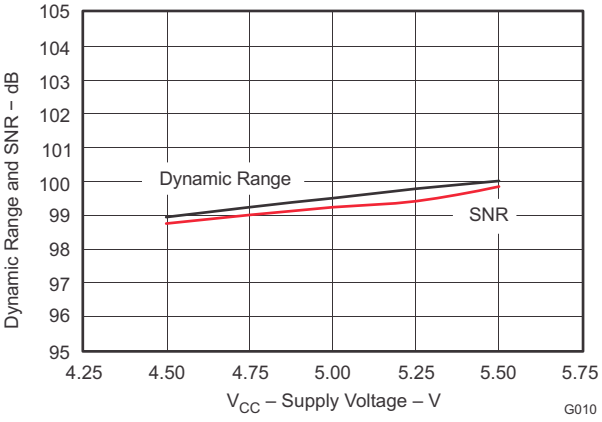

Figure 16. Dynamic Range and SNR vs Supply Voltage

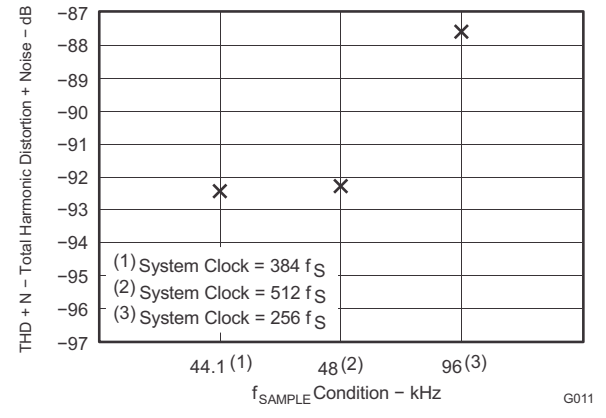

Figure 17. THD+N vs f_{SAMPLE} Condition

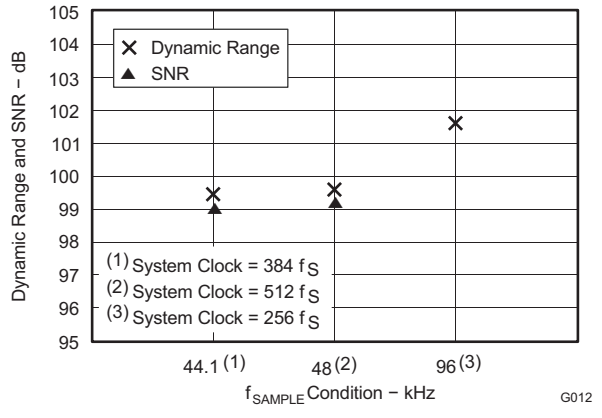

Figure 18. Dynamic Range and SNR vs f_{SAMPLE} Condition

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Typical Characteristics (continued)

All specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, master mode, f_S = 48 kHz, system clock = 512 f_S, 24-bit data, unless otherwise noted.

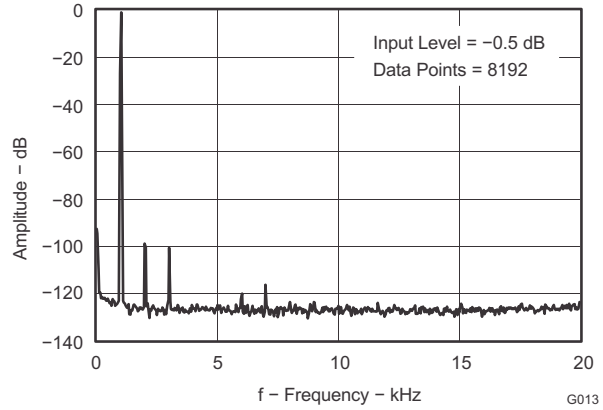


Figure 19. Output Spectrum (–0.5 dB, N = 8192)

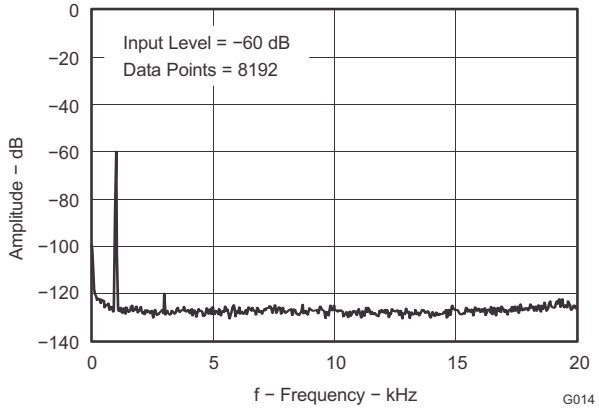


Figure 20. Output Spectrum (–60 dB, N = 8192)

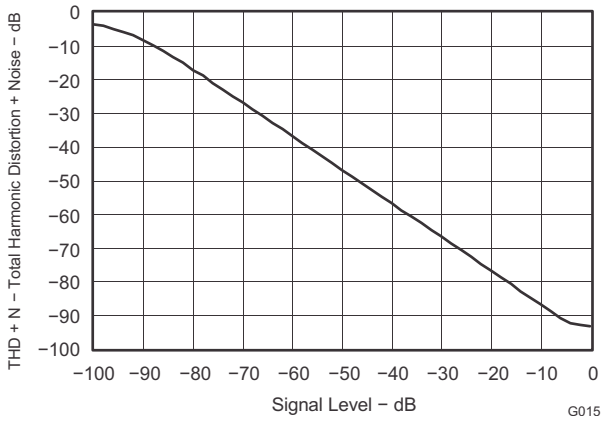


Figure 21. Output Spectrum THD+N vs Signal Level

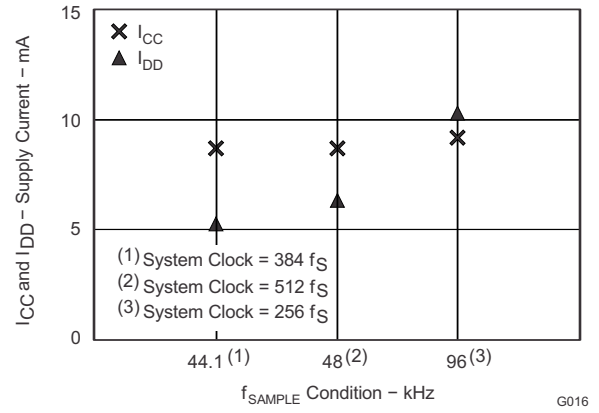


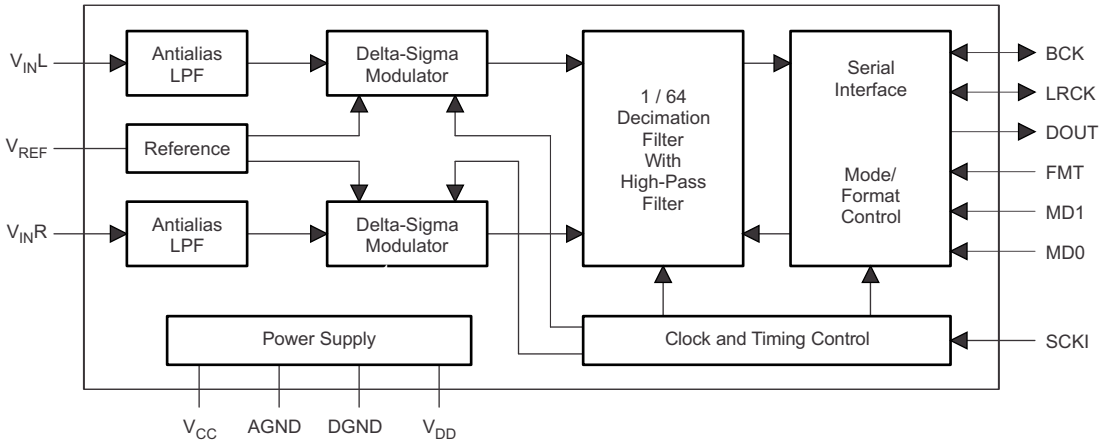
Figure 22. Supply Current vs f_{SAMPLE} Condition

7 Detailed Description

7.1 Overview

The PCM1808 is high-performance, low-cost, single-chip, stereo analog-to-digital converter with single-ended analog voltage input. The PCM1808 uses a delta-sigma modulator with 64-times oversampling and includes a digital decimation filter and high-pass filter that removes the dc component of the input signal. For various applications, the PCM1808 supports master and slave mode and two data formats in serial audio interface up to 96-kHz sampling. These features are controlled through hardware by pulling pins high or low with resistors or a controller GPIO. The PCM1808 also supports a power-down and reset function by means of halting the system clock.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Hardware Control

Pins FMT, MD0, and MD1 allow the device to be controlled by either pullup or pulldown resistors as well as GPIO from a digital IC. These controls allow the option of switching between I^2S or left-justified, and in which interface mode the device operates.

7.3.2 System Clock

The PCM1808 device supports 256 f_S, 384 f_S, and 512 f_S as system clock, where f_S is the audio sampling frequency. The system clock input must be on SCKI (pin 6).

The PCM1808 device has a system-clock detection circuit which automatically senses if the system-clock operation is at 256 f_S, 384 f_S, or 512 f_S in slave mode. In master mode, control of the system clock frequency must be through the serial control port, which uses MD1 (pin 11) and MD0 (pin 10). An internal circuit automatically divides down the system clock to generate frequencies of 128 f_S and 64 f_S, which operate the digital filter and the delta-sigma modulator, respectively.

Table 1 shows some typical relationships between sampling frequency and system clock frequency, and Figure 1 shows system clock timing.

Table 1. Sampling Frequency and System Clock Frequency

SAMPLING FREQUENCY (kHz)	SYSTEM CLOCK FREQUENCY (f_{SCLK}) (MHz)		
	256 f_S	384 f_S	512 f_S
8	2.048	3.072	4.096
16	4.096	6.144	8.192
32	8.192	12.288	16.384
44.1	11.2896	16.9344	22.5792

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Feature Description (continued)

Table 1. Sampling Frequency and System Clock Frequency (continued)

SAMPLING FREQUENCY (kHz)	SYSTEM CLOCK FREQUENCY (f_{SCLK}) (MHz)		
	256 f_S	384 f_S	512 f_S
48	12.288	18.432	24.576
64	16.384	24.576	32.768
88.2	22.5792	33.8688	45.1584
96	24.576	36.864	49.152

7.3.3 Synchronization With Digital Audio System

In slave mode, the PCM1808 device operates under LRCK (pin 7), synchronized with system clock SCKI (pin 6). The PCM1808 device does not require a specific phase relationship between LRCK and SCKI, but does require the synchronization of LRCK and SCKI.

If the relationship between LRCK and SCKI changes more than ±6 BCKs for 64 BCK/frame (±5 BCKs for 48 BCK/frame) during one sample period due to LRCK or SCKI jitter, internal operation of the ADC halts within 1 / f_S and digital output goes to zero data (BPZ code) until resynchronization between LRCK and SCKI occurs.

In the case of changes less than ±5 BCKs for 64 BCK/frame (±4 BCKs for 48 BCK/frame), resynchronization does not occur, and the previously described digital output control and discontinuity do not occur.

Figure 23 illustrates the digital output response for loss of synchronization and resynchronization. During undefined data, the PCM1808 device can generate some noise in the audio signal. Also, the transition of normal data to undefined data creates a discontinuity in the digital output data, which can generate some noise in the audio signal. The digital output is valid after resynchronization completes and the time of 32 / f_S has elapsed. Because the fade-in operation is performed, it takes additional time of 48 / f_{in} or 48 / f_S to obtain the level corresponding to the analog input signal. In the case of loss of synchronization during the fade-in or fade-out operation, the operation stops and DOUT (pin 9) goes to zero data immediately. The fade-in operation resumes from mute after the time of 32 / f_S following resynchronization.

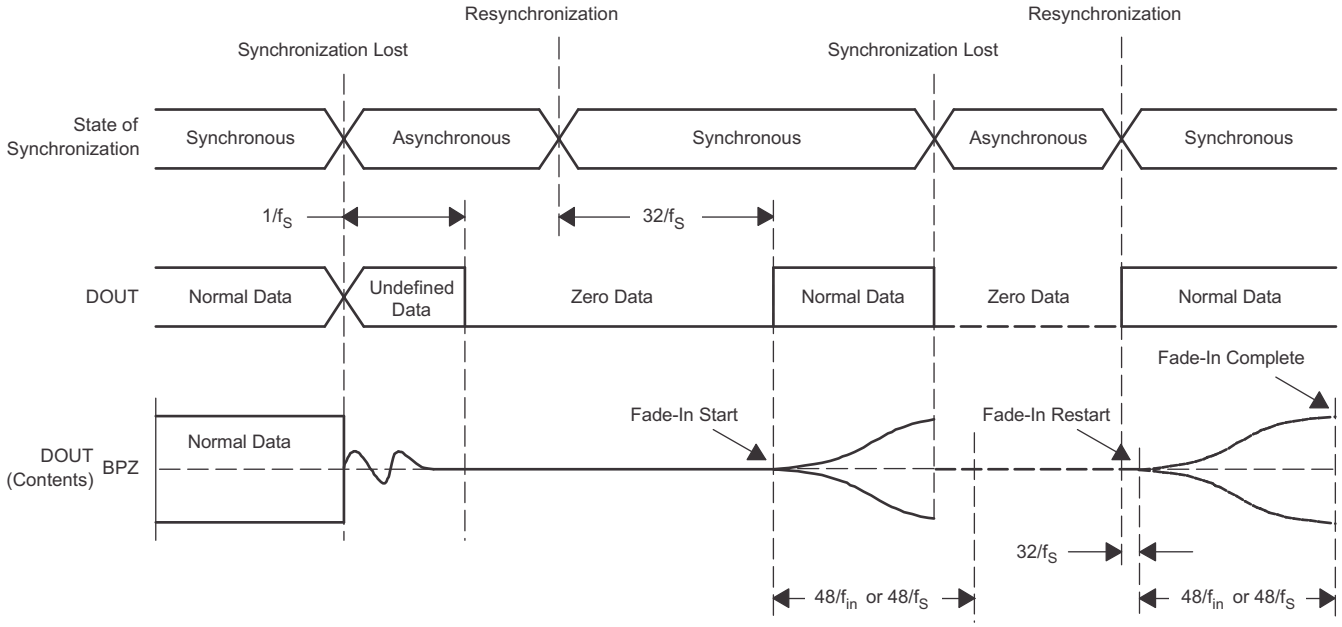

Figure 23. ADC Digital Output for Loss of Synchronization and Resynchronization

7.3.4 Power On

The PCM1808 device has an internal power-on-reset circuit, and initialization (reset) occurs automatically when the power supply (V_{DD}) exceeds 2.2 V (typical). While V_{DD} < 2.2 V (typical), and for 1024 system-clock counts after V_{DD} > 2.2 V (typical), the PCM1808 device stays in the reset state and the digital output remains zero. After release of the reset state, 8960 / f_S seconds must pass before the digital output becomes valid. Because of the performing of the fade-in operation, it takes additional time of 48 / f_{in} or 48 / f_S to obtain the data corresponding to the analog input signal. Figure 2 illustrates the power-on timing and the digital output.

7.3.5 Serial Audio Data Interface

The PCM1808 device interfaces the audio system through LRCK (pin 7), BCK (pin 8), and DOUT (pin 9).

7.3.5.1 Interface Mode

MD1 (pin 11) and MD0 (pin 10) select master mode and slave mode as interface modes, both of which the PCM1808 device supports.Table 2 shows the interface-mode selections. It is necessary to set MD1 and MD0 prior to power on.

In master mode, the PCM1808 device provides the timing of serial audio data communications between the PCM1808 device and the digital audio processor or external circuit. While in slave mode, the PCM1808 device receives the timing for data transfer from an external controller.

Table 2. Interface Modes

MD1 (PIN 11)	MD0 (PIN 10)	INTERFACE MODE
Low	Low	Slave mode (256 f_S, 384 f_S, 512 f_S autodetection)
Low	High	Master mode (512 f_S)
High	Low	Master mode (384 f_S)
High	High	Master mode (256 f_S)

7.3.5.1.1 Master Mode

In master mode, BCK and LRCK work as output pins, timing which from the clock circuit of the PCM1808 device controls these pins. The frequency of BCK is constant at 64 BCK/frame.

7.3.5.1.2 Slave Mode

In slave mode, BCK and LRCK work as input pins. The PCM1808 device accepts 64-BCK/frame or 48-BCK/frame format (only for a 384-f_S system clock), not 32-BCK/frame format.

7.3.5.2 Data Format

Table 3. Data Format

FORMAT NO.	FMT (Pin 12)	FORMAT
0	Low	I^2S, 24-bit
1	High	Left-justified, 24-bit

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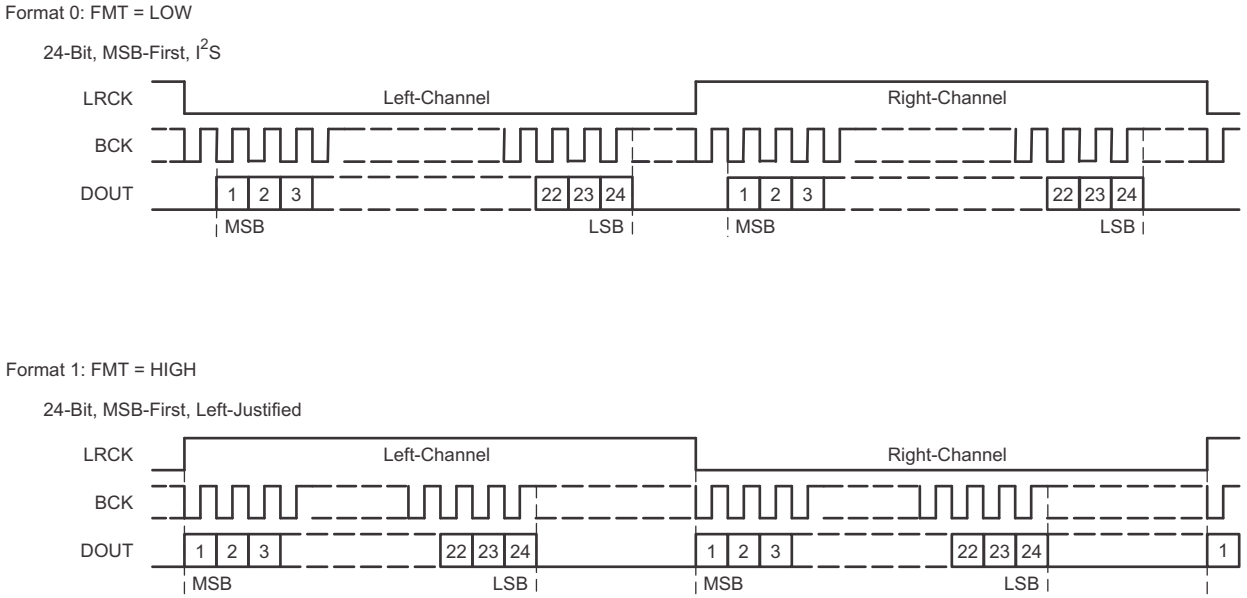

Figure 24. Audio Data Format (LRCK and BCK Work as Inputs in Slave Mode and as Outputs in Master Mode)

7.3.5.3 Interface Timing

Figure 4 and Figure 5 illustrate the interface timing in slave mode and master mode, respectively.

7.4 Device Functional Modes

7.4.1 Fade-In and Fade-Out Functions

The PCM1808 device has fade-in and fade-out functions on DOUT (pin 9) to avoid pop noise, and the functions come into operation in some cases as described in several following sections. Performance of the level changes from 0 dB to mute or mute to 0 dB employs calculated pseudo S-shaped characteristics with zero-cross detection. Because of the zero-cross detection, the time needed for the fade-in and fade-out depends on the analog input frequency (f_{in}). It takes 48 / f_{in} to complete the processing. If there is no zero-cross during 8192 / f_S, a forced DOUT fade-in or fade-out occurs during 48 / f_S (TIME OUT). Figure 25 illustrates the fade-in and fade-out operation processing.

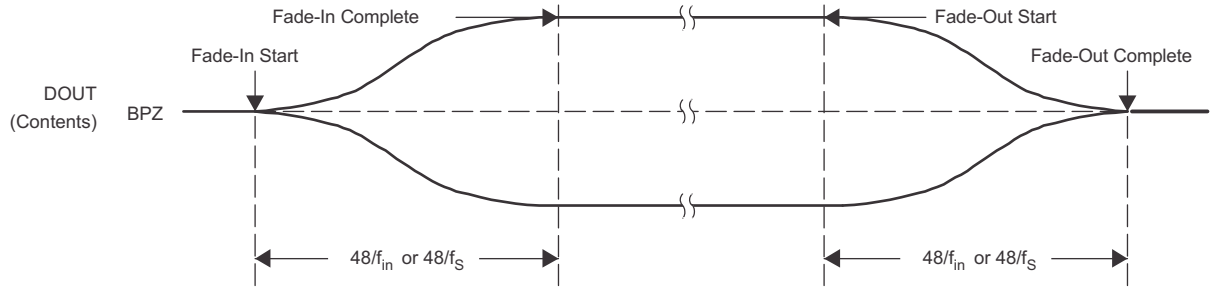

Figure 25. Fade-In and Fade-Out Operations

Device Functional Modes (continued)

7.4.2 Clock-Halt Power-Down and Reset Function

The PCM1808 device has a power-down and reset function. Halting SCKI (pin 6) in both master and slave modes triggers this function. The function is available any time after power on. Reset and power down occur automatically 4 µs (minimum) after the halt of SCKI. During assertion of the clock-halt reset, the PCM1808 device stays in the reset and power-down mode, with DOUT (pin 9) forced to zero. Release the reset and power-down mode requires the supply of SCKI. The digital output is valid after release of the reset state and elapse of the time of 1024 SCKI + 8960 / f_S. Performing the fade-in operation takes additional time of 48 / f_{in} or 48 / f_S to attain the level corresponding to the analog input signal. Figure 3 illustrates the clock-halt reset timing.

To avoid ADC performance degradation, BCK (pin 8) and LRCK (pin 7) must synchronize with SCKI within 4480 / f_S after the resumption of SCKI. If it takes more than 4480 / f_S for BCK and LRCK to synchronize with SCKI, mask SCKI until it again achieves synchronization, taking care of glitch and jitter. See the typical circuit connection diagram, Figure 26.

To avoid ADC performance degradation, assertion of the clock-halt reset is necessary when changing system clock SCKI or the audio interface clocks BCK and LRCK (sampling rate f_S) on the fly.

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8 Application and Implementation

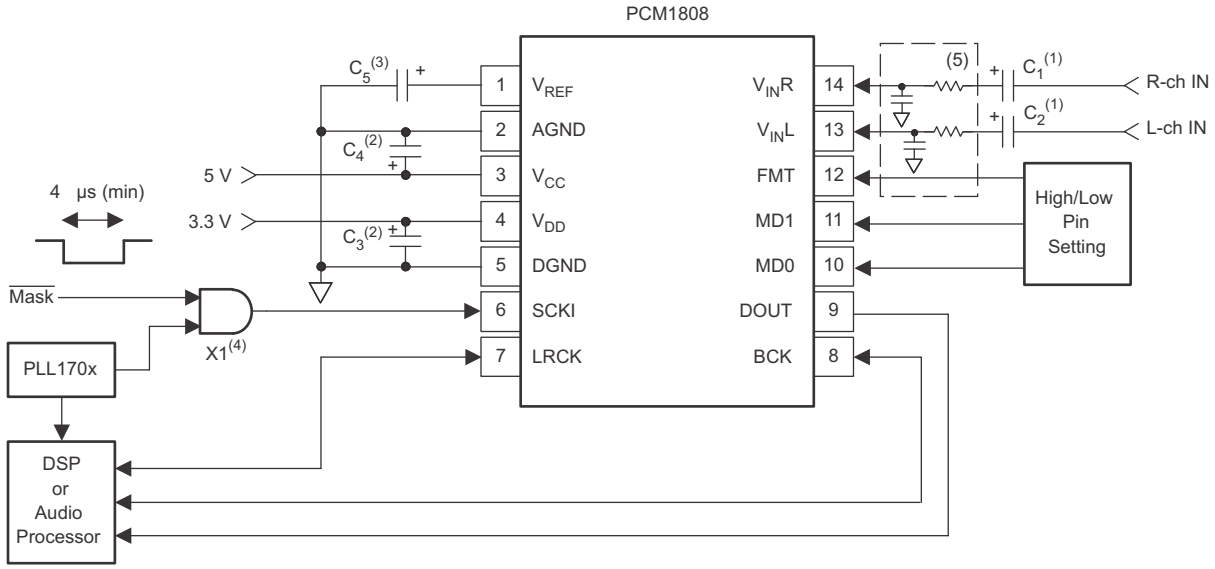
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The PCM1808 device is suitable for wide variety of cost-sensitive consumer applications requiring good performance and operation with a 5-V analog supply and 3.3-V digital supply.

8.2 Typical Application



(1) C1, C2: A 1-µF electrolytic capacitor gives 2.7 Hz (τ = 1 µF × 60 kΩ) cutoff frequency for the input HPF in normal operation and requires a power-on settling time with a 60-ms time constant in the power-on initialization period.

(2) C3, C4: Bypass capacitors, 0.1-µF ceramic and 10-µF electrolytic, depending on layout and power supply

(3) C5: Recommended capacitors are 0.1-µF ceramic and 10-µF electrolytic.

(4) X1: X1 masks the system clock input when using the clock-halt reset function with external control.

(5) Optional external antialiasing filter could be required, depending on the application.

Figure 26. Typical Circuit Connection Diagram

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 4 as the input parameters.

Table 4. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Analog input voltage range	0 Vp-p to 3 Vp-p
Output	PCM audio data
System clock input frequency	2.048 MHz to 49.152 MHz
Output sampling frequency	8 kHz to 96 kHz
Power supply	3.3 V and 5 V

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8.2.2 Detailed Design Procedure

8.2.2.1 Control Pins

The control pins FMT, MD0, and MD1 should be controlled either by biasing with a 10 kΩ resister to VDD or GND, or by driving with GPIO from the DSP or audio processor.

8.2.2.2 Master Clock

In this application of the PCM1808 device, a PLL170X series device is used as the master clock source to drive both the PCM1808 and the DSP or audio processor synchronously. With the addition of the AND gate, the operation of the PCM1808 device can be halted by control of the MASK bit. A crystal that operates at the standard audio multiples can also be used.

8.2.2.3 DSP or Audio Processor

In this application, the DSP or audio processor is acting as the audio master, and the PCM1808 is acting as the audio slave. This means the DSP or audio processor must be able to output audio clocks that the PCM1808 can use to process audio signals.

8.2.2.4 Input Filters

For the analog input circuit, an ac coupling capacitor should be placed in series with the input. This will remove the dc component of the input signal. An RC filter can also be implemented to filter out-of-band noise to reduce aliasing. The equation below can be used to calculate the cutoff frequency of the optional RC filter for the input.

$$f_C = \frac{1}{2\pi RC} \quad (1)$$

8.2.3 Application Curve

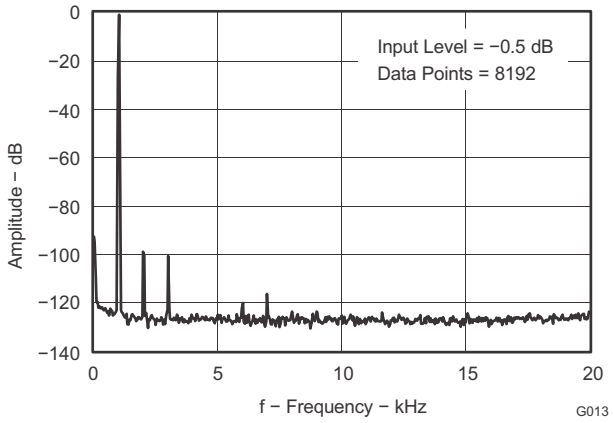

Figure 27. Output Spectrum

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9 Power Supply Recommendations

The PCM1808 device requires a 5-V nominal supply and a 3.3-V nominal supply. The 5-V supply is for the analog circuitry powered by the V_{CC} pin. The 3.3-V supply is for the digital circuitry powered by the V_{DD} pin. The decoupling capacitors for the power supplies should be placed close to the device terminals.

A V_{CC} that varies from the nominal 5 V affects the reference voltage for the input. This has a slight impact on the data conversion of the device.

10 Layout

10.1 Layout Guidelines

10.1.1 V_{CC}, V_{DD} Pins

Bypass the digital and analog power supply lines to the PCM1808 device to the corresponding ground pins with both 0.1-µF ceramic and 10-µF electrolytic capacitors as close to the pins as possible to maximize the dynamic performance of the ADC.

10.1.2 AGND, DGND Pins

To maximize the dynamic performance of the PCM1808 device, there are no internal connections to the analog and digital grounds. These grounds should have low impedance to avoid digital noise feedback into the analog ground. They should be connected directly to each other under the PCM1808 device package to reduce potential noise problems.

10.1.3 V_{IN}L, V_{IN}R Pins

V_{IN}L and V_{IN}R are single-ended inputs. These inputs have integrated antialias low-pass filters to remove the high-frequency noise outside the audio band. If the performance of these filters is not adequate for an application, the application requires appropriate external antialiasing filters. An appropriate choice would typically be a passive RC filter in the range of 100 Ω and 0.01 µF to 1 kΩ and 1000 pF.

10.1.4 V_{REF} Pin

To ensure low source impedance of the ADC references, the recommended capacitors between V_{REF} and AGND are 0.1-µF ceramic and 10-µF electrolytic. These capacitors should be located as close as possible to the V_{REF} pin to reduce dynamic errors on the ADC references.

10.1.5 DOUT Pin

The DOUT pin has a large load-drive capability, but if the DOUT line is long, a recommended practice is to locate a buffer near the PCM1808 device and minimize load capacitance to minimize the digital-analog crosstalk and maximize the dynamic performance of the ADC.

10.1.6 System Clock

The quality of the system clock can influence dynamic performance, as the PCM1808 device operates based on a system clock. Therefore, it may be necessary to consider the system clock duty, jitter, and the time difference between system clock transition and BCK or LRCK transition in slave mode.

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10.2 Layout Example

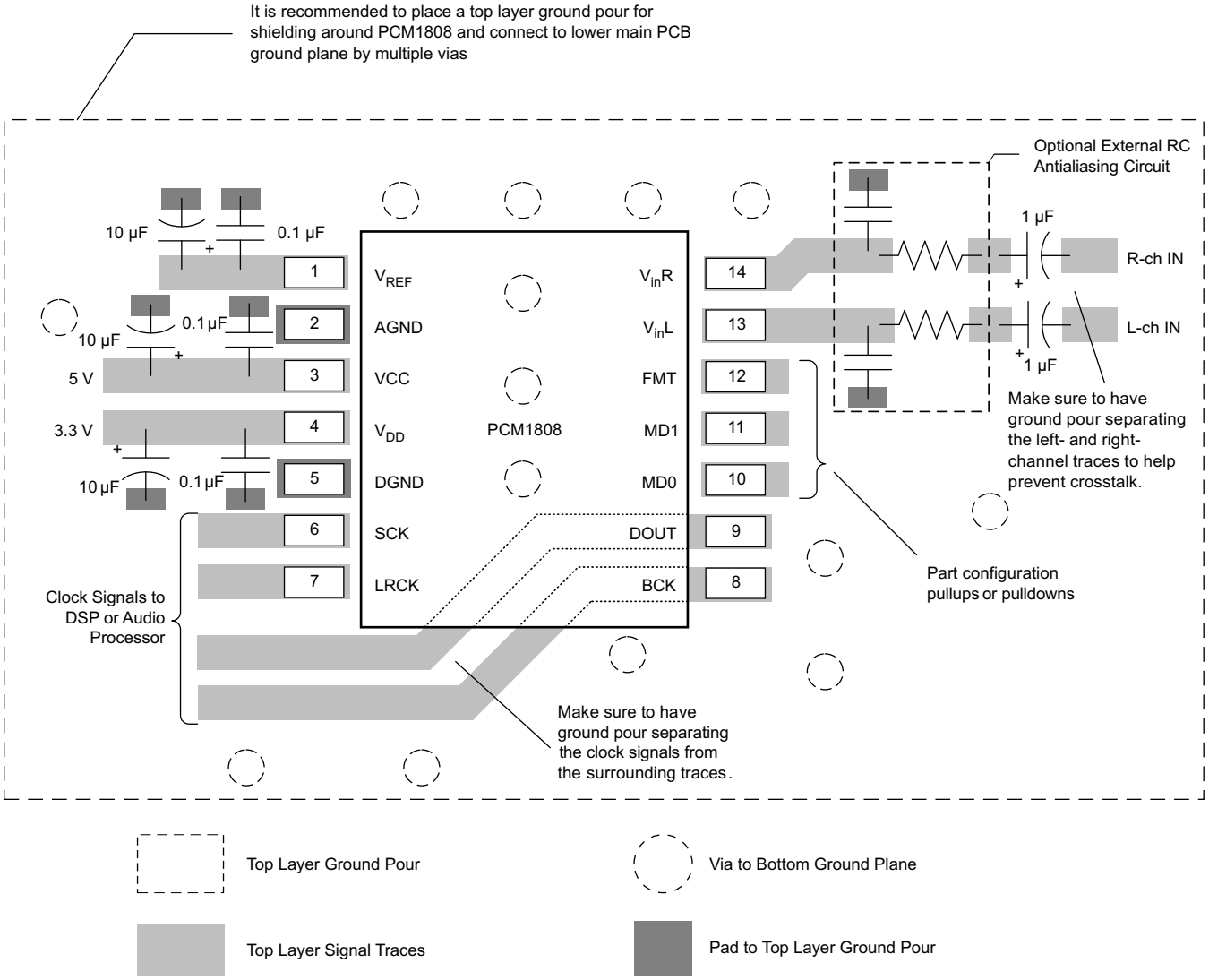

Figure 28. PCM1808 Layout Example

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11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
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All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCM1808PW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCM1808	Samples
PCM1808PWG4	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCM1808	Samples
PCM1808PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCM1808	Samples
PCM1808PWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCM1808	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF PCM1808 :

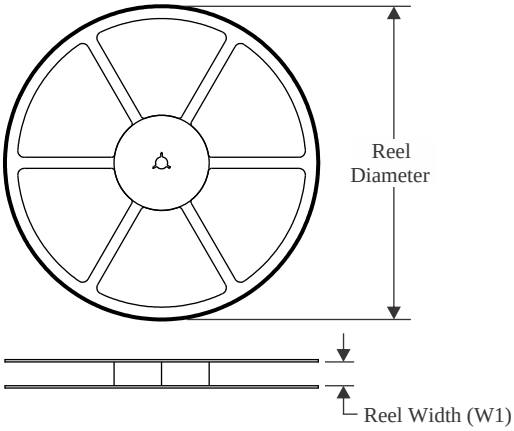
- Automotive: PCM1808-Q1

NOTE: Qualified Version Definitions:

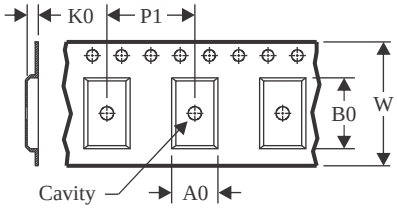
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

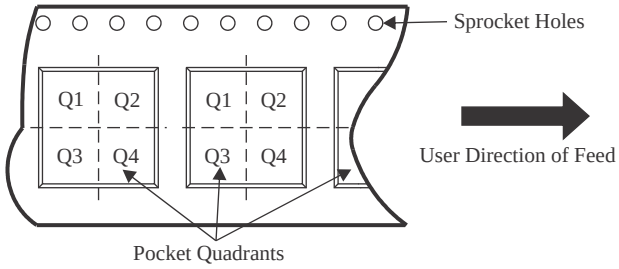


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

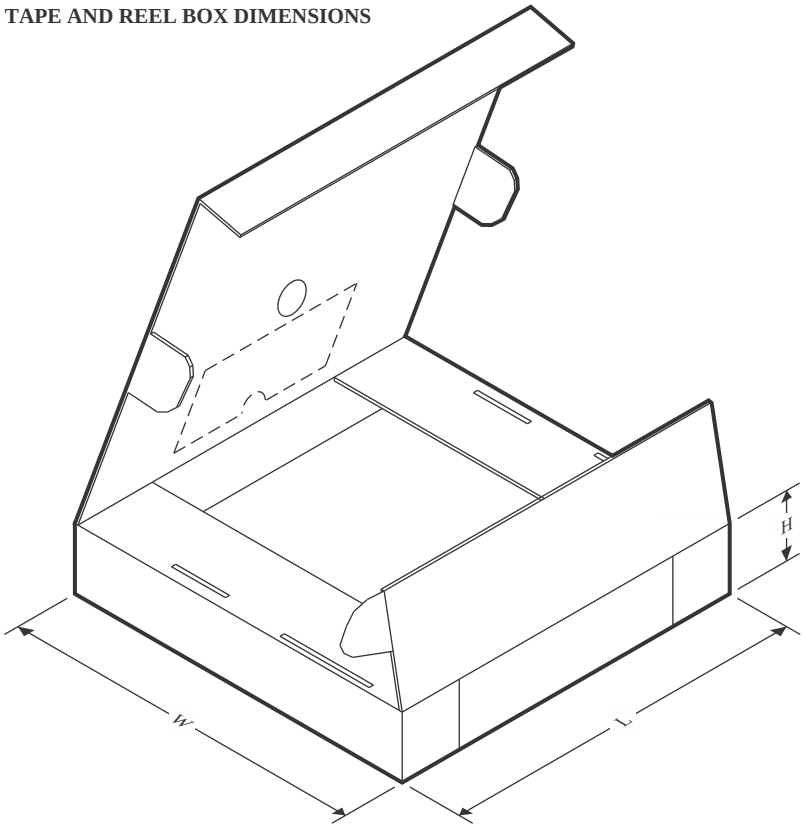
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM1808PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

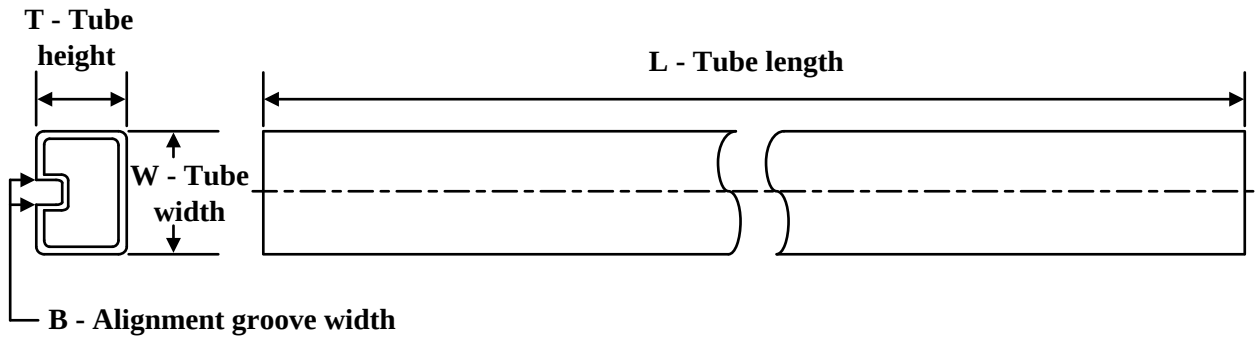
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM1808PWR	TSSOP	PW	14	2000	356.0	356.0	35.0

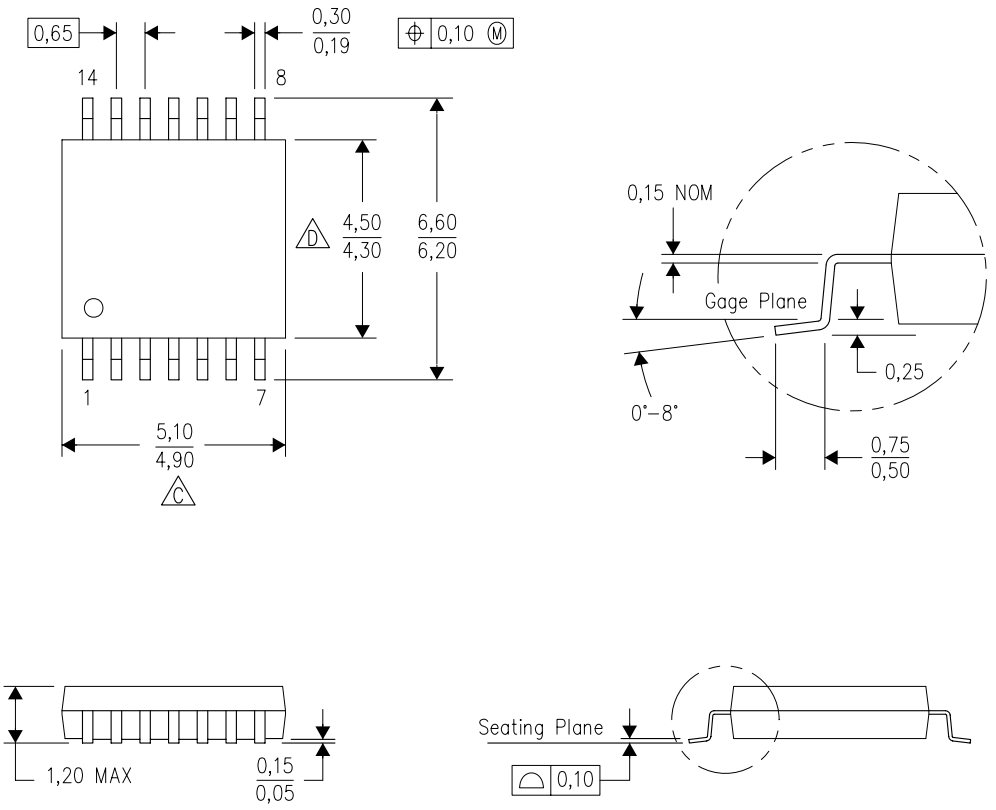
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
PCM1808PW	PW	TSSOP	14	90	530	10.2	3600	3.5
PCM1808PW	PW	TSSOP	14	90	530	10.2	3600	3.5
PCM1808PWG4	PW	TSSOP	14	90	530	10.2	3600	3.5
PCM1808PWG4	PW	TSSOP	14	90	530	10.2	3600	3.5

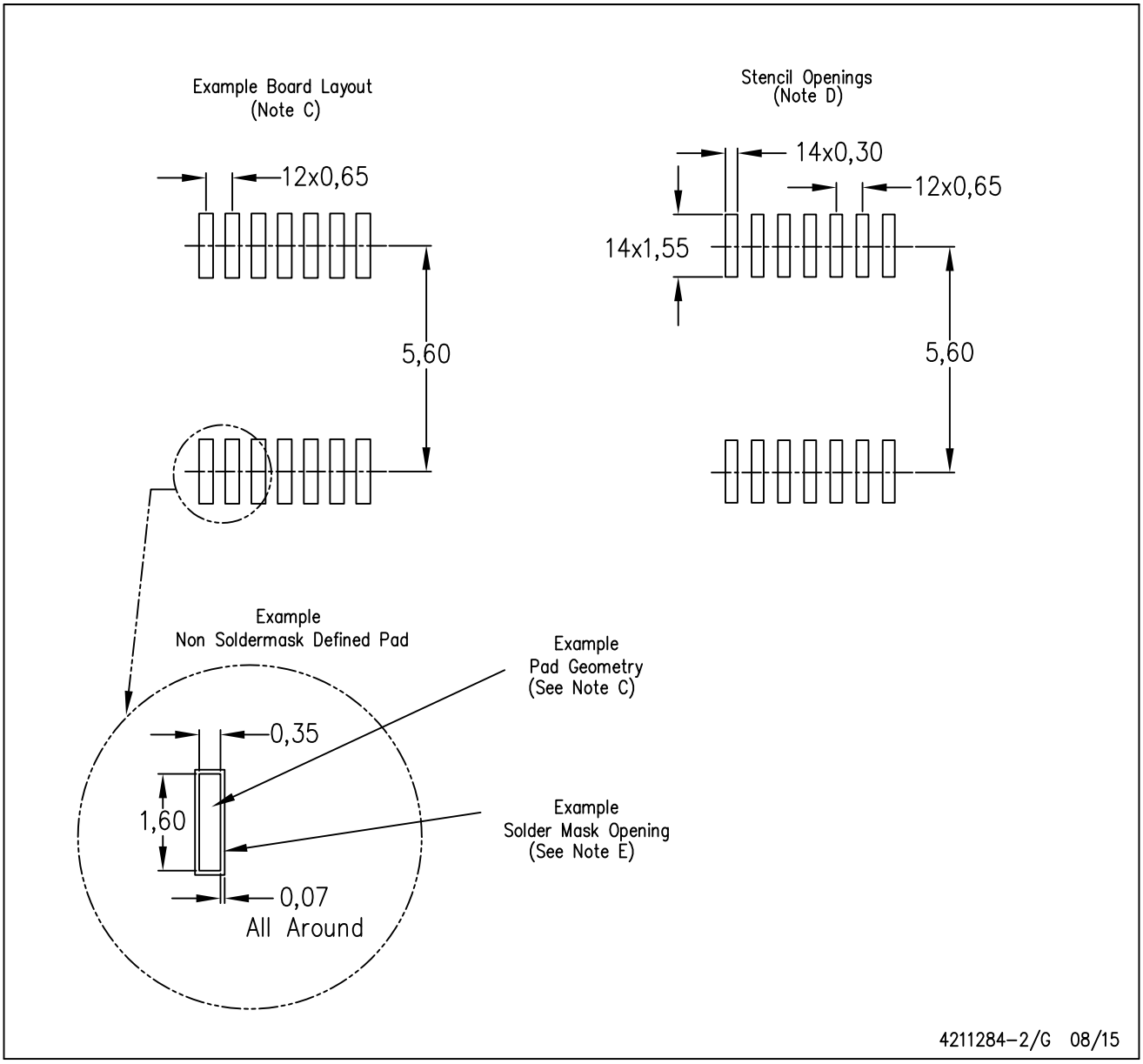
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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