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DP83902A

DP83902A ST-NIC(TM) Serial Network Interface Controller for Twisted Pair



Literature Number: SNLS082A

National Semiconductor

PRELIMINARY
November 1995

DP83902A ST-NIC™
Serial Network Interface Controller for Twisted Pair

Obsolete

General Description

The DP83902A Serial Network Interface Controller for Twisted Pair (ST-NIC) is a microCMOS VLSI device designed for easy implementation of CSMA/CD local area networks. These include Ethernet (10BASE5), Thin Ethernet (10BASE2) and Twisted-pair Ethernet (10BASE-T). The overall ST-NIC solution provides the Media Access Control (MAC) and Encode-Decode (ENDEC) with an AUI interface, and 10BASE-T transceiver functions in accordance with the IEEE 802.3 standards.

The DP83902A's 10BASE-T transceiver fully complies with the IEEE standard. This functional block incorporates the receiver, transmitter, collision, heartbeat, loopback, jabber, and link integrity blocks as defined in the standard. The transceiver when combined with equalization resistors, transmit/receive filters, and pulse transformers provides a complete physical interface from the DP83902A's ENDEC module and the twisted pair medium.

The integrated ENDEC module allows Manchester encoding and decoding via a differential transceiver and phase lock loop decoder at 10 Mbit/sec. Also included are collision detect translator and diagnostic loopback capability. The ENDEC module interfaces directly to the transceiver module, and also provides a fully IEEE compliant AUI (Attachment Unit Interface) for connection to other media transceivers.

(Continued)

Features

- Single chip solution for IEEE 802.3, 10BASE-T
- Integrated controller, ENDEC, and transceiver
- Full AUI interface
- No external precision components required
- 3 levels of loopback supported

Transceiver Module

- Integrates transceiver electronics, including:
  - — Transmitter and receiver
  - — Collision detect, heartbeat and jabber timer
  - — Link integrity test
- Link disable and polarity detection/correction
- Integrated smart receive squelch
- Reduced squelch level for extended distance cable operation (100-pin QFP version)

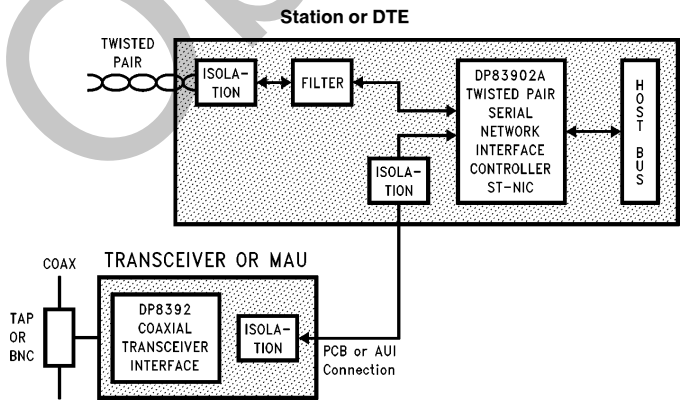
ENDEC Module

- 10 Mb/s Manchester encoding/decoding, plus clock recovery
- Transmitter half or full step mode
- Squelch on receive and collision pairs
- Lock time 5 bits typical
- Decodes Manchester data with up to ±18 ns jitter

MAC/Controller Module

- 100% DP8390 software/hardware compatible
- Dual 16-bit DMA channels
- 16-byte internal FIFO
- Efficient buffer management implementation
- Independent system and network clocks
- Supports physical, multicast and broadcast address filtering
- Network statistics storage

1.0 System Diagram



TL/F/11157–1

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General Description (Continued)

The Media Access Control function which is provided by the Network Interface Control module (NIC) provides simple and efficient packet transmission and reception control by means of unique dual DMA channels and an internal FIFO. Bus arbitration and memory control logic are integrated to reduce board cost and area overheads.

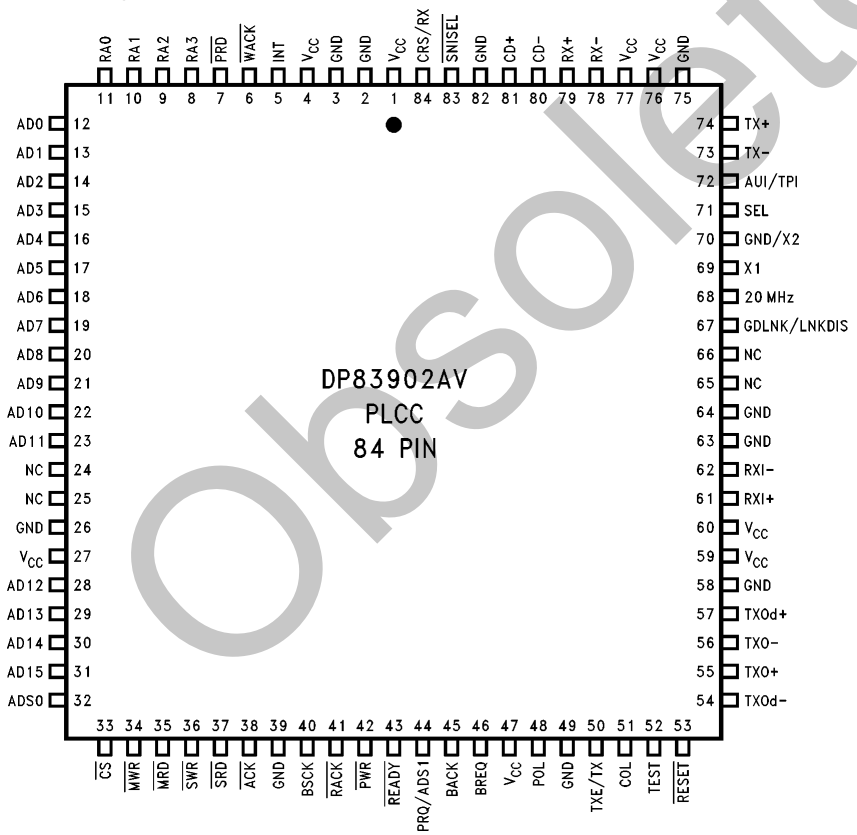
DP83902A provides a comprehensive single chip solution for 10BASE-T IEEE 802.3 networks and is designed for easy interface to other transceivers via the AUI interface.

Due to the inherent constraints of CMOS processing, isolation is required at the AUI differential signal interface for 10BASE5 and 10BASE2 applications. Capacitive or inductive isolation may be used.

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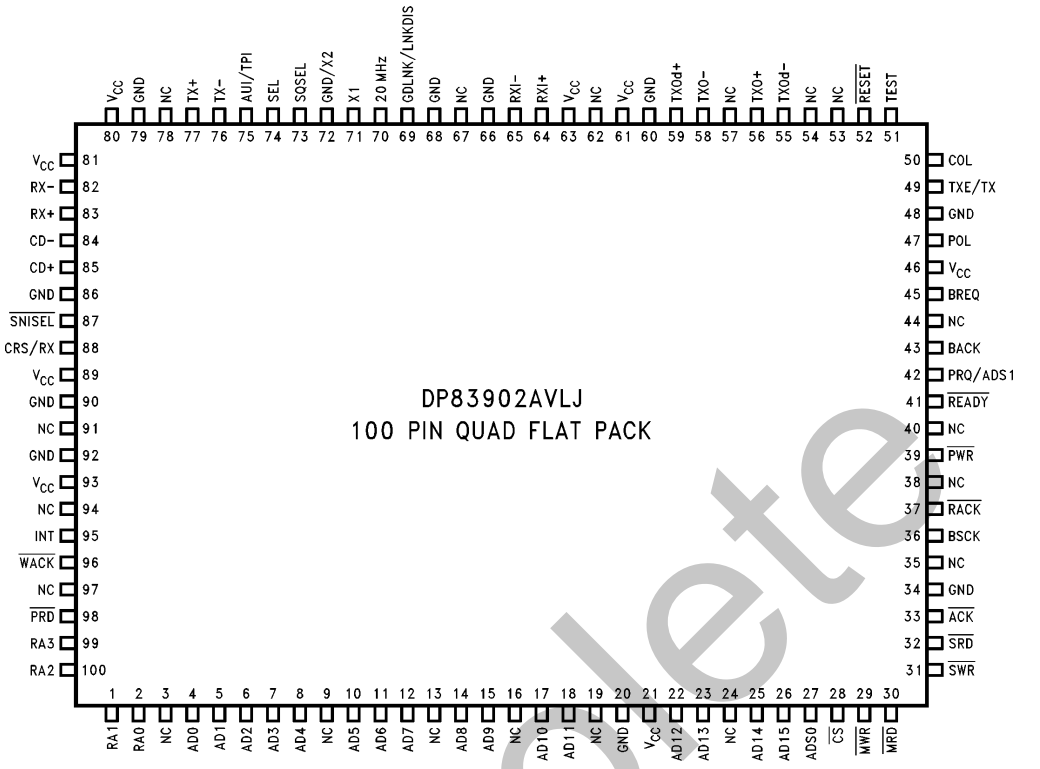


TL/F/11157–2

Order Number DP83902AV
See NS Package Number V84A

Obsolete

Connection Diagrams (Continued)

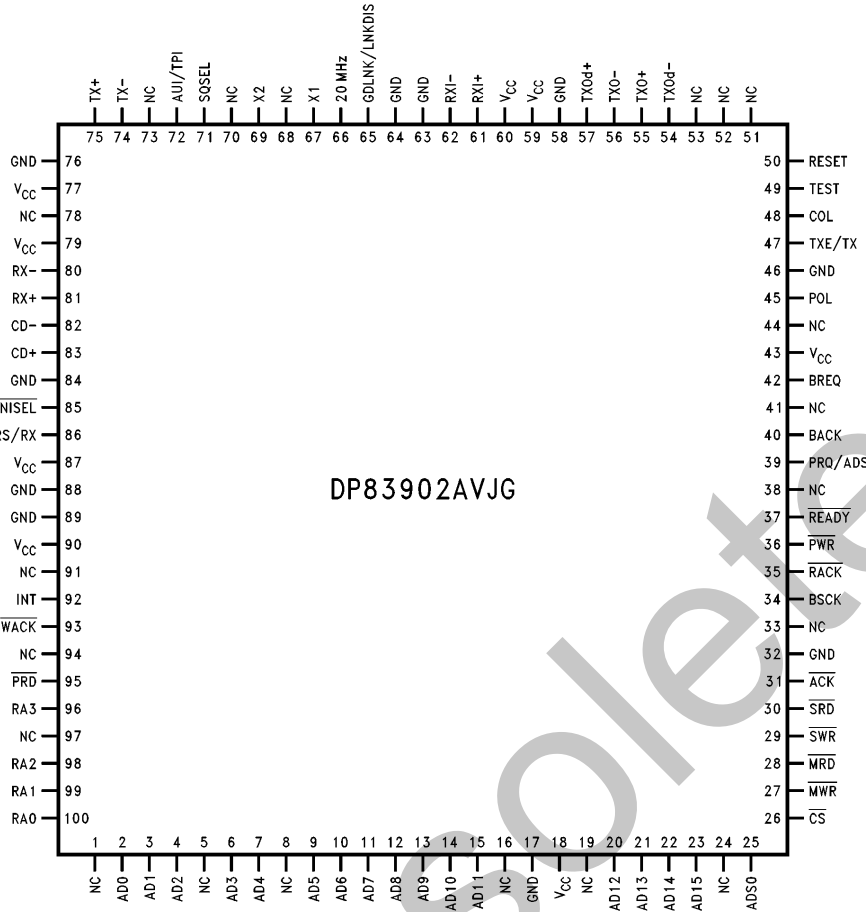


TL/F/11157–56

Order Number DP83902AVLJ
See NS Package Number VLJ100A

Obsolete

Connection Diagrams (Continued)



TL/F/11157–65

Order Number DP83902AVJG
See NS Package Number VJG100A

2.0 Pin Description

PQFP Pin No.	PLCC Pin No.	AVJG Pin No.	Pin Name	I/O	Description
BUS INTERFACE PINS					
95	5	92	INT	O	**INTERRUPT:** Indicates that the DP83902A requires CPU attention after reception transmission or completion of DMA transfers. The interrupt is cleared by writing to the ISR (Interrupt Status Register). All interrupts are maskable.
96	6	93	$\overline{\text{WACK}}$	I	**WRITE ACKNOWLEDGE:** Issued from system to DP83902A to indicate that data has been written to the external latch. The DP83902A will begin a write cycle to place the data in local memory.
98	7	95	$\overline{\text{PRD}}$	O	**PORT READ:** Enables data from external latch on to local bus during a memory write cycle to local memory (remote write operation). This allows asynchronous transfer of data from the system memory to local memory.
99, 100, 1, 2	8–11	96, 98–100	RA3–RA0	I	**REGISTER ADDRESS:** These four pins are used to select a register to be read or written. The state of these inputs is ignored when the DP83902A is not in slave mode ($\overline{\text{CS}}$ high).

Obsolete

2.0 Pin Description (Continued)

PQFP Pin No.	PLCC Pin No.	AVJG Pin No.	Pin Name	I/O	Description
BUS INTERFACE PINS (Continued)					
4–8, 10–12, 14, 15, 17, 18, 22, 23, 25, 26	12–23, 28–31	2–4, 6, 7, 9–15, 20–23	AD0–AD15	I/O, Z	**MULTIPLEXED ADDRESS/DATA BUS:** • Register Access, with DMA inactive, $\overline{CS}$ low and $\overline{ACK}$ returned from DP83902A, pins AD0–AD7 are used to read and write register data. AD8–AD15 float during I/O transfers, $\overline{SRD}$, $\overline{SWR}$ pins are used to select direction of transfer. • Bus Master with BACK input asserted. During t1 of memory cycle AD0–AD15 contain address. During t2, t3, t4 AD0–AD15 contain data (word transfer mode). During t2, t3, t4 AD0–AD7 contain data, AD8–AD15 contain address (byte transfer mode). Direction of transfer is indicated by DP83902A on $\overline{MWR}$, $\overline{MRD}$ lines.
27	32	25	ADS0	I/O, Z	**ADDRESS STROBE 0:** • Input: with DMA inactive and $\overline{CS}$ low, latches RA0–RA3 inputs on falling edge. If high, data present on RA0–RA3 will flow through latch. • Output: When Bus Master, latches address bits (AD0–AD15) to external memory during DMA transfers.
28	33	26	$\overline{CS}$	I	**CHIP SELECT:** Chip Select places controller in slave mode for μP access to internal registers. Must be valid through data portion of bus cycle. RA0–RA3 are used to select the internal register. $\overline{SWR}$ and $\overline{SRD}$ select direction of data transfer.
29	34	27	$\overline{MWR}$	O, Z	**MASTER WRITE STROBE:** (Strobe for DMA transfers) Active low during write cycles (t2, t3, tw) to buffer memory. Rising edge coincides with the presence of valid output data. TRI-STATE® until BACK asserted.
30	35	28	$\overline{MRD}$	O, Z	**MASTER READ STROBE:** (Strobe for DMA transfers) Active during read cycles (t2, t3, tw) to buffer memory. Input data must be valid on rising edge of MRD. TRI-STATE until BACK asserted.
31	36	29	$\overline{SWR}$	I	**SLAVE WRITE STROBE:** Strobe from CPU to write an internal register selected by RA0–RA3. Data is latched into the DP83902A on the rising edge of this input.
32	37	30	$\overline{SRD}$	I	**SLAVE READ STROBE:** Strobe from CPU to read an internal register selected by RA0–RA3. The register data is output when $\overline{SRD}$ goes low.
33	38	31	$\overline{ACK}$	O	**ACKNOWLEDGE:** Active low when DP83902A grants access to CPU. Used to insert WAIT states to CPU until DP83902A is synchronized for a register read or write operation.
36	40	34	BSCK	I	**BUS CLOCK:** This clock is used to establish the period of the DMA memory cycle. Four clock cycles (t1, t2, t3, t4) are used per DMA cycle. DMA transfers can be extended by one BSCK increment using the $\overline{READY}$ input.
37	41	35	$\overline{RACK}$	I	**READ ACKNOWLEDGE:** Indicates that the system DMA or host CPU has read the data placed in the external latch by the DP83902A. The DP83902A will begin a read cycle to update the latch.
39	42	36	$\overline{PWR}$	O	**PORT WRITE:** Strobe used to latch data from the DP83902A into external latch for transfer to host memory during Remote Read transfers. The rising edge of $\overline{PWR}$ coincides with the presence of valid data on the local bus.
41	43	37	$\overline{READY}$	I	**READY:** This pin is set high to insert wait states during a DMA transfer. The DP83902A will sample this signal at t3 during DMA transfers.
42	44	39	PRQ/ ADS1	O, Z	**PORT REQUEST/ADDRESS STROBE 1** • 32-BIT MODE: If LAS is set in the Data Configuration Register, this line is programmed as ADS1. It is used to strobe addresses A16–A31 into external latches. (A16–A31 are the fixed addresses stored in RSAR0, RSAR1). ADS1 will remain at TRI-STATE until BACK is received. • 16-BIT MODE: If LAS is not set in the Data Configuration Register, this line is programmed as PRQ and is used for Remote DMA Transfers. The DP83902A initiates a single remote DMA read or write operation by asserting this pin. In this mode PRQ will be a standard logic output. **Note:** This line will power up as TRI-STATE until the Data Configuration Register is programmed.

Obsolete

2.0 Pin Description (Continued)

PQFP Pin No.	PLCC Pin No.	AVJG Pin No.	Pin Name	I/O	Description
BUS INTERFACE PINS (Continued)					
43	45	40	BACK	I	**BUS ACKNOWLEDGE:** Bus Acknowledge is an active high signal indicating that the CPU has granted the bus to the DP83902A. If immediate bus access is desired, BREQ should be tied to BACK. **Tying BACK to V_{CC} will result in a deadlock.**
45	46	42	BREQ	O	**BUS REQUEST:** Bus Request is an active high signal used to request the bus for DMA transfers. This signal is automatically generated when the FIFO needs servicing.
52	53	50	$\overline{\text{RESET}}$	I	**RESET:** Reset is active low and places the DP83902A in a reset mode immediately. No packets are transmitted or received by the DP83902A until STA bit is set. Affects Command Register, Interrupt Mask Register, Data Configuration Register and Transmit Configuration Register. The DP83902A will execute reset within 10 BSCK cycles.
NETWORK INTERFACE PINS					
47	48	45	POL	O	**POLARITY:** A TTL/MOS active high output. This signal is normally in the low state. When the TPI module detects seven consecutive link pulses or three consecutive received packets with reversed polarity POL, is asserted.
49	50	47	TXE/TX	O	**TRANSMIT ENABLE/TRANSMIT:** A TTL/MOS active high output. It is asserted for approximately 50 ms whenever the DP83902A transmits data in either AUI or TPI modes.
50	51	48	COL	O	**COLLISION:** A TTL/MOS active high output. It is asserted for approximately 50 ms whenever the DP83902A detects a collision in either the AUI or TPI modes.
51	52	49	TEST	I	**FACTORY TEST INPUT:** Used to check the chip's internal functions. This should be tied low during normal operation.
55, 56, 58, 59	54, 55, 56, 57	54, 55, 56, 57	TXOd−, TXO+, TXO−, TXOd+	O	**TWISTED PAIR TRANSMIT OUTPUTS:** These high drive CMOS level outputs are resistively combined external to the chip to produce a differential output signal with equalization to compensate for Intersymbol Interference (ISI) on the twisted pair medium.
64, 65	61, 62	61, 62	RXI+, RXI−	I	**TWISTED PAIR RECEIVE INPUTS:** These inputs feed a differential amplifier which passes valid data to the ENDEC module.
69	67	65	GDLNK/ LNKDIS	I/O	**GOOD LINK/LINK DISABLE:** This pin has a dual function both input and output. The function is latched by the DP83902A on the rising edge of the Reset signal i.e.: on the chip returning to normal operation after reset. As an output this pin is configured as an open drain N-channel device and is suitable for driving a LED. It will be latched as output on removal of chip reset if connected to a LED or left open circuit. Under normal conditions (the twisted pair link is not broken) the output will be low, and the LED will be lit. The open drain output will be switched off if the twisted pair link has been detected to be broken. It is recommended that the color of the LED be green. This output will be pulled high in AUI mode, by an internal resistor of approximately 15 kΩ. When this pin, which has an internal pull-up resistor to V_{DD}, is tied low it becomes an input and the link integrity checking is disabled.
73	—	70	SQSEL	I	**TPI SQUELCH SELECT:** This pin selects the TPI module input squelch thresholds. When tied low, the input squelch threshold on the RXI± inputs complies to 10BASE-T specification. When set high, the RXI± input operates with reduced squelch levels, allowing its use with longer lengths of cable or cable with higher losses. If this pin is left unconnected, an internal pulldown causes the ST-NIC's TPI to default to the higher squelch level.
70	68	66	20 MHz	O	**20 MHz:** This is a TTL/MOS level signal. It is a buffered version of the oscillator X2. It is suitable to drive external logic.
71	69	67	X1	I	**EXTERNAL OSCILLATOR INPUT**
72	70	69	GND/ X2	I	**GROUND/X2:** If an oscillator is used, this pin should be tied to ground and if a crystal is used, this pin should be tied directly to the crystal.
74	71	71	SEL	I	**MODE SELECT:** When high, TX+ and TX− are the same voltage in the idle state. When low, Transmit+ is positive with respect to Transmit− in the idle state, at the transformer's primary.

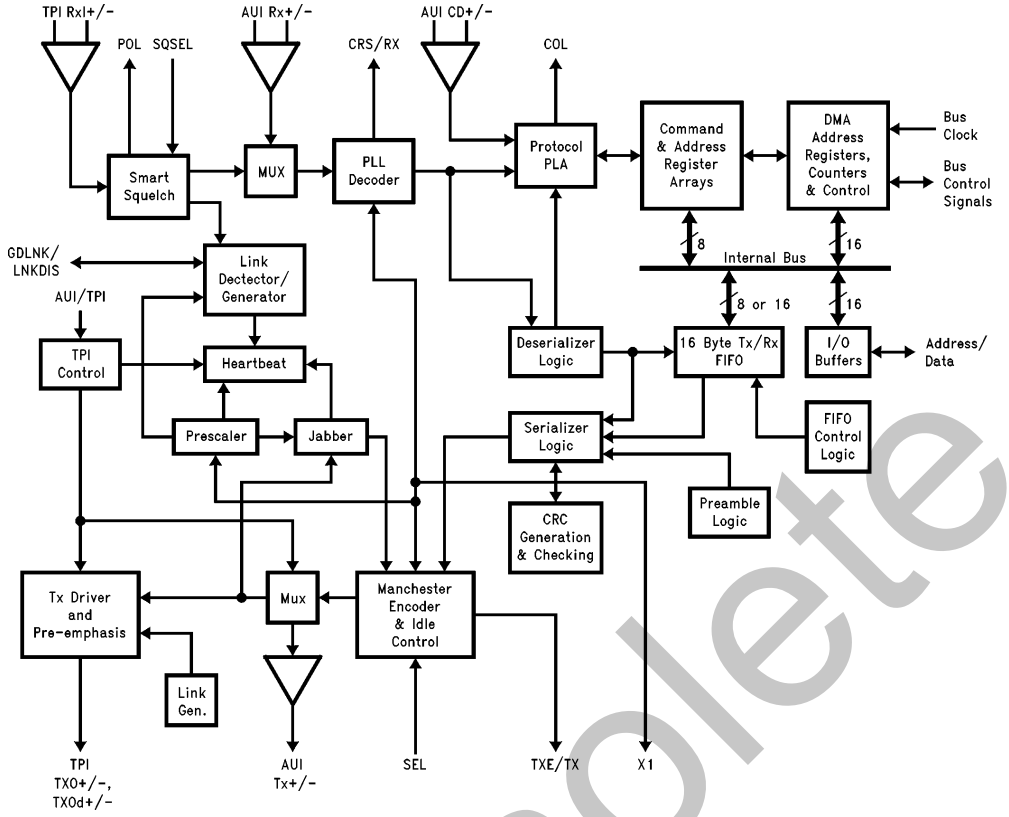
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2.0 Pin Description (Continued)

PQFP Pin No.	PLCC Pin No.	AVJG Pin No.	Pin Name	I/O	Description
NETWORK INTERFACE PINS (Continued)					
75	72	72	AUI/ TPI	I	**AUI/TPI SELECT:** A TTL level active high input that selects either the AUI interface or the TPI module for interface with the ENDEC module. When high the AUI is selected, when low the TPI is selected.
76, 77	73, 74	74, 75	TX−, TX+	O	**AUI TRANSMIT OUTPUT:** Differential driver which sends the encoded data to the transceiver. The outputs are source followers which require 270Ω pulldown resistors.
82, 83	78, 79	80, 81	RX−, RX+	I	**AUI RECEIVE INPUT:** Differential receive input pair from the transceiver.
84, 85	80, 81	82, 83	CD−, CD+	I	**AUI COLLISION INPUT:** Differential collision pair input from the transceiver.
87	83	85	$\overline{\text{SNISEL}}$	I	**FACTORY TEST INPUT:** For normal operation tied to V_{CC}. When low enables the ENDEC module to be tested independently of the DP83902A module.
88	84	86	CRS/ RX	O	**CARRIER SENSE/RECEIVE:** A TTL/MOS level active high signal. It is asserted for approximately 50 ms whenever valid transmit or receive data is detected while in AUI mode or receive data is detected while in TPI mode.
POWER SUPPLY PINS (DIGITAL)					
21, 46, 89	1, 27, 47	18, 43, 87	V_{CC}		**POSITIVE 5V SUPPLY PINS**
20, 34, 48, 68, 90	2, 26, 39, 49, 64	17, 32, 46, 64, 88	GND		**NEGATIVE (GROUND) SUPPLY PINS:** It is suggested that a decoupling capacitor be connected between the V_{CC} and GND pins.
POWER SUPPLY PINS (ANALOG)					
93	4	90	V_{CC}		**VCO 5V SUPPLY PIN:** Care should be taken to reduce noise on this pin as it supplies power to the analog VCO to the Phase Lock Loop.
92	3	89	GND		**VCO GROUND SUPPLY PIN:** Care should be taken to reduce noise on this pin as it supplies ground to the analog VCO to the Phase Lock Loop.
63	60	60	V_{CC}		**TPI RECEIVE 5V SUPPLY:** Power pin supplies 5V to the Twisted Pair Interface Receiver.
66	63	63	GND		**TPI RECEIVE GROUND:** Ground pin for the Twisted Pair Interface Receiver.
61	59	59	V_{CC}		**TPI TRANSMIT 5V SUPPLY:** Power pin supplies 5V to the Twisted Pair Interface Transmitter.
60	58	58	GND		**TPI TRANSMIT GROUND:** Ground pin for the Twisted Pair Interface Transmitter.
81	77	79	V_{CC}		**AUI RECEIVE 5V SUPPLY:** Power pin supplies 5V to the AUI Interface Receiver.
86	82	84	GND		**AUI RECEIVE GROUND:** Ground pin for the AUI Interface Receiver.
80	76	77	V_{CC}		**AUI TRANSMIT 5V SUPPLY:** Power pin supplies 5V to AUI Interface Transmitter.
79	75	76	GND		**AUI TRANSMIT GROUND:** Ground pin for the AUI Interface Transmitter.
NO CONNECTION					
3, 9, 13, 16, 19, 24, 35, 38, 40, 44, 53, 54, 57, 62, 67, 78, 91, 94, 97	24, 25, 65, 66	1, 5, 8, 16, 19, 24, 33, 38, 41, 44, 51, 52, 53, 68, 70, 73, 78, 91, 94, 97	NC		NO CONNECTION. Do not connect to these pins.

Obsolete

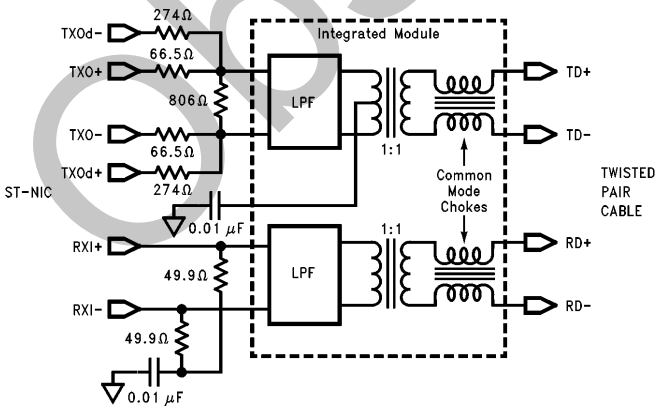
3.0 Block Diagram



TL/F/11157–3

FIGURE 1

Typical Connection to Twisted Pair Cable



TL/F/11157–4

Recommended integrated modules are:
1) Pulse Engineering PE65431
2) Belfuse 0556-2006-01 or 0556-3392-00
3) Valor FL1012.

ST-NIC Twisted Pair Interface

Obsolete

4.0 Functional Description (Refer to *Figure 1*)

TWISTED PAIR INTERFACE (TPI) MODULE

The TPI consists of five main logical functions:

a) The Smart Squelch, responsible for determining when valid data is present on the differential receive inputs (RXI±).

b) The Collision function checks for simultaneous transmission and reception of data on the TXO± and RXI± pins.

c) The Link Detector/Generator checks the integrity of the cable connecting the two twisted pair MAUs.

d) The Jabber disables the transmitter if it attempts to transmit a longer than legal packet.

e) The Tx Driver & Pre-emphasis transmits Manchester encoded data to the twisted pair network via the summing resistors and transformer/filter.

SMART SQUELCH

The ST-NIC implements an intelligent receive squelch on the RXI± differential inputs to ensure that impulse noise on the receive inputs will not be mistaken for a valid signal.

The squelch circuitry employs a combination of amplitude and timing measurements to determine the validity of data on the twisted pair inputs. There are two squelch levels which are selectable via the SQSEL pin. One mode is 10BASE-T compatible, and the second is reduced squelch mode.

The diagram shows the 10BASE-T mode operation of the smart squelch.

The signal at the start of packet is checked by the smart squelch and any pulses not exceeding the squelch level (either positive or negative, depending upon polarity) will be rejected. Once this first squelch level is overcome correctly the opposite squelch level must then be exceeded within 150 ns. Finally the signal must exceed the original squelch level within a further 150 ns to ensure that the input waveform will not be rejected. The checking procedure results in the loss of typically three bits at the beginning of each packet.

Only after all these conditions have been satisfied will a control signal be generated to indicate to the remainder of the circuitry that valid data is present. At this time the smart squelch circuitry is reset.

Valid data is considered to be present until either squelch level has not been generated for a time longer than 150 ns, indicating End of Packet. Once good data has been detected the squelch levels are reduced to minimize the effect of noise causing premature End of Packet detection.

The reduced squelch mode functions the same as the 10BASE-T mode except that only the lower level is used for both turn-on and turn-off.

COLLISION

A collision is detected by the TPI module when the receive and transmit channels are active simultaneously. If the TPI is receiving when a collision is detected it is reported to the controller immediately. If, however, the TPI is transmitting when a collision is detected the collision is not reported until seven bits have been received while in the collision state. This prevents a collision being reported incorrectly due to noise on the network. The signal to the controller remains for the duration of the collision.

Approximately 1 μs after the transmission of each packet a signal called the Signal Quality Error (SQE) consisting of typically 10 cycles of 10 MHz is generated. This 10 MHz signal, also called the Heartbeat, ensures the continued functioning of the collision circuitry.

LINK DETECTOR/GENERATOR

The link generator is a timer circuit that generates a link pulse as defined by the 10BASE-T specification that will be generated by the transmitter section. The pulse which is 100 ns wide is transmitted on the TXO+ output, every 16 ms, in the absence of transmit data.

The pulse is used to check the integrity of the connection to the remote MAU. The link detection circuit checks for valid pulses from the remote MAU and if valid link pulses are not received the link detector will disable the transmit, receive and collision detection functions.

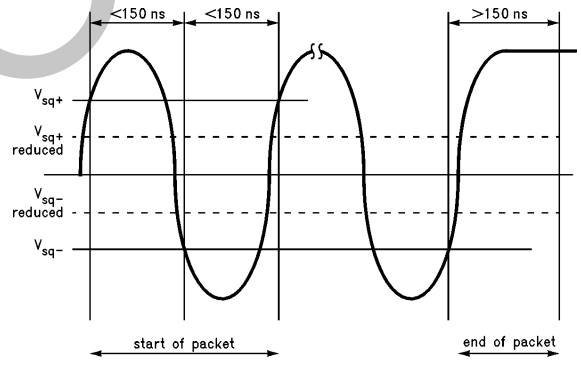
The GDLNK output can directly drive a LED to show that there is a good twisted pair link. For normal conditions the LED will be on. The link integrity function can be disabled as described in the Pin Description Section.

JABBER

The jabber timer monitors the transmitter and disables the transmission if the transmitter is active for greater than 26 ms. The transmitter is then disabled for the whole time that the ENDEC module's internal transmit enable is asserted. This signal has to be deasserted for approximately 750 ms (the unjab time) before the Jabber re-enables the transmit outputs.

TRANSMIT DRIVER

The transmitter consists of four signals, the true and complement Manchester encoded data (TXO±) and these signals delayed by 50 ns (TXOd±).



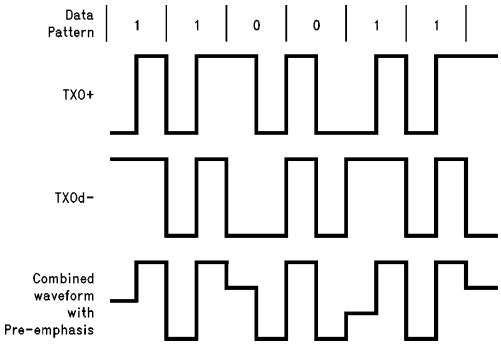
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4.0 Functional Description (Continued)

These four signals are resistively combined, TXO+ with TXOd− and TXO− with TXOd+. This is known as digital pre-emphasis and is required to compensate for the twisted pair cable which acts like a low pass filter causing greater attenuation to the 10 MHz (50 ns) pulses of the Manchester encoded waveform than the 5 MHz (100 ns) pulses.

An example of how these signals are combined is shown in the following diagram.



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The signal with pre-emphasis shown above is generated by resistively combining TXO+ and TXOd−. This signal along with its complement is passed to the transmit filter.

STATUS INFORMATION

Status information is provided by the ST-NIC on the CRS/RX, TXE/TX, COL and POL outputs as described in the pin description table. These outputs are suitable for driving status LEDs via an appropriate driver circuit.

The POL output is normally low, and will be driven high when seven consecutive link pulses or three consecutive receive packets are detected with reversed polarity. A polarity reversal can be caused by a wiring error at either end of the TPI cable. On detection of a polarity reversal the condition is latched and POL is asserted. The TPI corrects for this error internally and will decode received data correctly, eliminating the need to correct the wiring error.

ENCODER/DECODER (ENDEC) MODULE

The ENDEC consists of three main logical blocks:

a) The Manchester encoder accepts NRZ data from the controller, encodes the data to Manchester, and transmits it differentially to the transceiver, through the differential transmit driver.

b) The Manchester decoder receives Manchester data from the transceiver, converts it to NRZ data and clock pulses, and sends it to the controller.

c) The collision translator indicates to the controller the presence of a valid 10 MHz collision signal to the PLL.

MANCHESTER ENCODER AND DIFFERENTIAL DRIVER

The differential transmit pair, on the secondary of the transformer, drives up to 50 meters of twisted pair AUI cable. These outputs are source followers which require two 270Ω pull-down resistors to ground.

The DP83902A allows both half-step and full-step to be compatible with Ethernet and IEEE 802.3. With the SEL pin low (for Ethernet I). Transmit+ is positive with respect to Transmit− during idle; with SEL high (for IEEE 802.3), Transmit+ and Transmit− are equal in the idle state. This provides zero differential voltage to operate with transformer coupled loads.

MANCHESTER DECODER

The decoder consists of a differential receiver and a PLL to separate a Manchester decoded data stream into internal clock signals and data. The differential input must be externally terminated with two 39Ω resistors connected in series if the standard 78Ω transceiver drop cable is used. In thin Ethernet applications, these resistors are optional. To prevent noise from falsely triggering the decoder, a squelch circuit at the input rejects signals with levels less than −175 mV. Signals more negative than −300 mV are decoded. Data becomes valid typically within 5 bit times. The DP83902A may tolerate bit jitter up to 18 ns in the received data. The decoder detects the end of a frame when no more mid-bit transitions are detected.

COLLISION TRANSLATOR

When in AUI mode, when the Ethernet transceiver (DP8392 CTI) detects a collision, it generates a 10 MHz signal to the differential collision inputs (CD±) of the DP83902A. When these inputs are detected active, the DP83902A uses this signal to back off its current transmission and reschedule another one.

The collision differential inputs are terminated the same way as the differential receive inputs. The squelch circuitry is also similar, rejecting pulses with levels less than −175 mV.

CRYSTAL/OSCILLATOR OPERATION

OCSILLATOR

The oscillator is controlled by a 20 MHz parallel resonant crystal connected between X1 and X2 or by an external clock on X1. The 20 MHz output of the oscillator is divided by 2 to generate the 10 MHz transmit clock for the controller. The oscillator also provides internal clock signals to the encoding and decoding circuits.

Note: When X1 is being driven by an external oscillator, X2 MUST be grounded.

Crystal Specifications

Resonant Frequency	20 MHz
Tolerance	±0.005% at 25°C
Stability	±0.005% at 0°C–70°C
Type	AT Cut
Circuit	Parallel Resonance
Max ESR	25Ω
Crystal Load Capacitor	20 pF

The 20 MHz crystal connection to the DP83902 requires special care. The IEEE 802.3 standard requires the transmitted signal frequency to be accurate within ±0.01%. Stray capacitance can shift the crystal's frequency out of range and cause transmitted frequency to exceed its 0.01% tolerance. The frequency marked on the crystal is usually measured with a fixed load capacitance specified in the crystal's data sheet, typically 20 pF.

Obsolete

4.0 Functional Description (Continued)

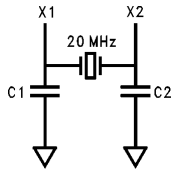
In order to prevent distortion on the transmitted frequency, the total capacitance seen by the crystal should equal the total load capacitance. On a standard parallel set-up as shown in the diagram below, the 2 load caps C1 and C2 should equal 2C1, the spec load cap, (due to the capacitors acting in series) less any stray capacitances.

Thus the trim capacitors required can be calculated as follows:

C1 = 2XC1 − (Cb1 + Cd1) Where Cb1 = Board cap on X1 and Cd1 = X1 dev cap

C2 = 2XC1 − (Cb2 + Cd2) Where Cb2 = Board cap on X2 and Cd2 = X2 dev cap

The value of STNIC pins X1 and X2 is in the region of 5 pF.



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NIC (Media Access Control) MODULE

RECEIVE DESERIALIZER

The Receive Deserializer is activated when the input signal Carrier Sense is asserted to allow incoming bits to be shifted into the shift register by the receive clock. The serial receive data is also routed to the CRC generator/checker. The Receive Deserializer includes a synch detector which detects the SFD (Start of Frame Delimiter) to establish where byte boundaries within the serial bit stream are located. After every eight receive clocks, the byte wide data is transferred to the 16-byte FIFO and the Receive Byte Count is incremented. The first six bytes after the SFD are checked for valid comparison by the Address Recognition Logic. If the Address Recognition Logic does not recognize the packet, the FIFO is cleared.

CRC GENERATOR/CHECKER

During transmission, the CRC logic generates a local CRC field for the transmitted bit sequence. The CRC encodes all fields after the SFD. The CRC is shifted out MSB first following the last transmit byte. During reception the CRC logic generates a CRC field from the incoming packet. This local CRC is serially compared to the incoming CRC appended to the end of the packet by the transmitting node. If the local and received CRC match, a specific pattern will be generated and decoded to indicate no data errors. Transmission errors result in different pattern and are detected, resulting in rejection of a packet (if so programmed).

TRANSMIT SERIALIZER

The Transmit Serializer reads parallel data from the FIFO and serializes it for transmission. The serializer is clocked by the transmit clock generated internally. The serial data is also shifted into the CRC generator/checker. At the beginning of each transmission, the Preamble and Synch Generator append 62 bits of 1,0 preamble and a 1,1 synch pattern. After the last data byte of the packet has been serialized the 32-bit FCS field is shifted directly out of the CRC generator. In the event of a collision the Preamble and Synch generators are used to generate a 32-bit JAM pattern of all 1's.

ADDRESS RECOGNITION LOGIC

The address recognition logic compares the Destination Address Field (first 6 bytes of the received packet) to the Physical address registers stored in the Address Register Array. If any one of the six bytes does not match the pre-programmed physical address, the Protocol Control Logic rejects the packet. All multicast destination addresses are filtered using a hashing technique. (See register description.) If the multicast address indexes a bit that has been set in the filter bit array of the Multicast Address Register Array the packet is accepted, otherwise it is rejected by the Protocol Control Logic. Each destination address is also checked for all 1's which is the reserved broadcast address.

FIFO AND BUS OPERATIONS

Overview

To accommodate the different rates at which data comes from (or goes to) the network and goes to (or comes from) the system memory, the ST-NIC contains a 16-byte FIFO for buffering data between the media. The FIFO threshold is programmable. When the FIFO has filled to its programmed threshold, the local DMA channel transfers these bytes (or words) into local memory. It is crucial that the local DMA is given access to the bus within a minimum bus latency time; otherwise a FIFO underrun (or overrun) occurs.

FIFO underruns or overruns are caused by two conditions: (1) the bus latency is so long that the FIFO has filled (or emptied) from the network before the local DMA has serviced the FIFO and (2) the bus latency has slowed the throughput of the local DMA to a point where it is slower than the network data rate (10 Mbit/sec). This second condition is also dependent upon DMA clock and word width (byte wide or word wide). The worst case condition ultimately limits the overall bus latency which the ST-NIC can tolerate.

Beginning of Receive

At the beginning of reception, the ST-NIC stores the entire Address field of each incoming packet in the FIFO to determine whether the address matches the ST-NIC's Physical Address Registers or maps to one of its Multicast Registers. This causes the FIFO to accumulate 8 bytes. Furthermore, there are some synchronization delays in the DMA PLA. Thus, the actual time to when BREQ is asserted from the time the Start of Frame Delimiter (SFD) is detected is 7.8 μs. This operation affects the bus latencies at 2- and 4-byte thresholds during the first receive BREQ since the FIFO must be filled to 8 bytes (or 4 words) before issuing a BREQ.

End of Receive

When the end of a packet is detected by the ENDEC module, the ST-NIC enters its end of packet processing sequence, emptying its FIFO and writing the status information at the beginning of the packet. The ST-NIC holds onto the bus for the entire sequence. The longest time BREQ may be extended occurs when a packet ends just as the ST-NIC performs its last FIFO burst. The ST-NIC, in this case, performs a programmed burst transfer followed by flushing the remaining bytes in the FIFO, and completes by writing the header information to memory. The following steps occur during this sequence.

1. ST-NIC issues BREQ because the FIFO threshold has been reached.
2. During the burst, packet ends, resulting in BREQ extended.

OBSOLETE

4.0 Functional Description (Continued)

3. ST-NIC flushes remaining bytes from FIFO.
4. ST-NIC performs internal processing to prepare for writing the header.
5. ST-NIC writes 4-byte (2-word) header.
6. ST-NIC de-asserts BREQ.

FIFO Threshold Detection

To assure that no overwriting of data in the FIFO, the FIFO logic flags a FIFO overrun as the 13th byte is written into the FIFO, effectively shortening the FIFO to 13 bytes. The FIFO logic also operates differently in Byte Mode and in Word Mode. In Byte Mode, a threshold is indicated when the n+1 byte has entered the FIFO; thus, with an 8-byte threshold, the ST-NIC issues Bus Request (BREQ) when the 9th byte has entered the FIFO. For Word Mode, BREQ is not generated until n+2 bytes have entered the FIFO. Thus, with a 4 word threshold (equivalent to an 8-byte threshold), BREQ is issued when the 10th byte has entered the FIFO.

Beginning of Transmit

Before transmitting, the ST-NIC performs a prefetch from memory to load the FIFO. The number of bytes prefetched is the programmed FIFO threshold. The next BREQ is not issued until after the ST-NIC actually begins transmitting data, i.e., after SFD.

Reading the FIFO

During normal operation, the FIFO must not be read. The ST-NIC will not issue an ACKnowledge back to the CPU if the FIFO is read. The FIFO should only be read during loopback diagnostics.

PROTOCOL PLA

The protocol PLA is responsible for implementing the IEEE 802.3 protocol, including collision recovery with random backoff. The Protocol PLA also formats packets during transmission and strips preamble and synch during reception.

DMA AND BUFFER CONTROL LOGIC

The DMA and Buffer Control Logic is used to control two 16-bit DMA channels. During reception, the local DMA stores packets in a receive buffer ring, located in buffer memory. During transmission the Local DMA uses programmed pointer and length registers to transfer a packet from local buffer memory to the FIFO. A second DMA channel is used as a slave DMA to transfer data between the local buffer memory and the host system. The Local DMA and Remote DMA are internally arbitrated, with the Local DMA channel having highest priority. Both DMA channels use a common external bus clock to generate all required bus timing. External arbitration is performed with a standard bus request, bus acknowledge handshake protocol.

5.0 Transmit/Receive Packet Encapsulation/Decapsulation

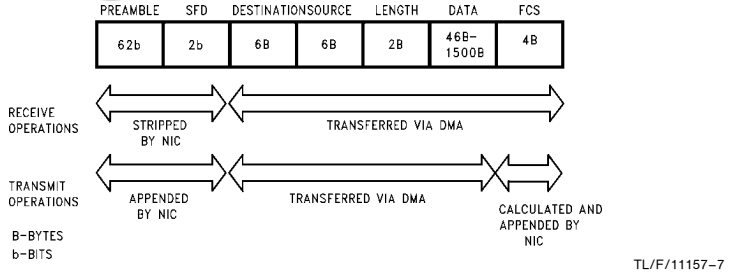
A standard IEEE 802.3 packet consists of the following fields: preamble, Start of Frame Delimiter (SFD), destination address, source address, length, data, and Frame Check Sequence (FCS). The typical format is shown in *Figure 2.* The packets are Manchester encoded and decoded by the ENDEC module and transferred serially to the NIC module using NRZ data with a clock. All fields are of fixed length except for the data field. The ST-NIC generates and appends the preamble, SFD and FCS field during transmission. The Preamble and SFD fields are stripped during reception. (The CRC is passed through to buffer memory during reception.)

PREAMBLE AND START OF FRAME DELIMITER (SFD)

The Manchester encoded alternating 1,0 preamble field is used by the ENDEC to acquire bit synchronization with an incoming packet. When transmitted each packet contains 62 bits of alternating 1,0 preamble. Some of this preamble will be lost as the packet travels through the network. The preamble field is stripped by the NIC module. Byte alignment is performed with the Start of Frame Delimiter (SFD) pattern which consists of two consecutive 1's. The ST-NIC does not treat the SFD pattern as a byte, it detects only the two bit pattern. This allows any preceding preamble within the SFD to be used for phase locking.

DESTINATION ADDRESS

The destination address indicates the destination of the packet on the network and is used to filter unwanted packets from reaching a node. There are three types of address formats supported by the ST-NIC: physical, multicast and broadcast. The physical address is a unique address that corresponds only to a single node. All physical addresses have an MSB of "0". These addresses are compared to the internally stored physical address registers. Each bit in the destination address must match in order for the ST-NIC to accept the packet. Multicast addresses begin with an MSB of "1". The ST-NIC filters multicast addresses using a standard hashing algorithm that maps all multicast addresses into a 6-bit value. This 6-bit value indexes a 64-bit array that filters the value. If the address consists of all 1's it is a broadcast address, indicating that the packet is intended for all nodes. A promiscuous mode allows reception of all packets: the destination address is not required to match any filters. Physical, broadcast, multicast, and promiscuous address modes can be selected.



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FIGURE 2

Obsolete

5.0 Transmit/Receive Packet Encapsulation/Decapsulation
(Continued)

SOURCE ADDRESS

The source address is the physical address of the node that sent the packet. Source addresses cannot be multicast or broadcast addresses. This field is simply passed to buffer memory.

LENGTH/TYPE FIELD

The 2-byte length field indicates the number of bytes that are contained in the data field of the packet. This field is not interpreted by the ST-NIC.

DATA FIELD

The data field consists of anywhere from 46 to 1500 bytes. Messages longer than 1500 bytes need to be broken into multiple packets. Messages shorter than 46 bytes will require appending a pad to bring the data field to the minimum length of 46 bytes. If the data field is padded, the number of valid data bytes is indicated in the length field. **The ST-NIC does not strip or append pad bytes for short packets, or check for oversize packets.**

FCS FIELD

The Frame Check Sequence (FCS) is a 32-bit CRC field calculated and appended to a packet during transmission to allow detection of errors when a packet is received. During reception, error free packets result in a specific pattern in the CRC generator. Packets with improper CRC will be rejected. The AUTODIN II ($X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X^1 + 1$) polynomial is used for the CRC calculations.

6.0 Direct Memory Access Control (DMA)

The DMA capabilities of the ST-NIC greatly simplify the use of the DP83902A in typical configurations. The local DMA channel transfers data between the FIFO and memory. On transmission, the packet is DMAed from memory to the FIFO in bursts. Should a collision occur (up to 15 times), the packet is retransmitted with no processor intervention. On reception, packets are DMAed from the FIFO to the receive buffer ring (as explained below).

dA remote DMA channel is also provided on the ST-NIC to accomplish transfers between a buffer memory and system memory. The two DMA channels can alternatively be combined to form a single 32-bit address with 8- or 16-bit data.

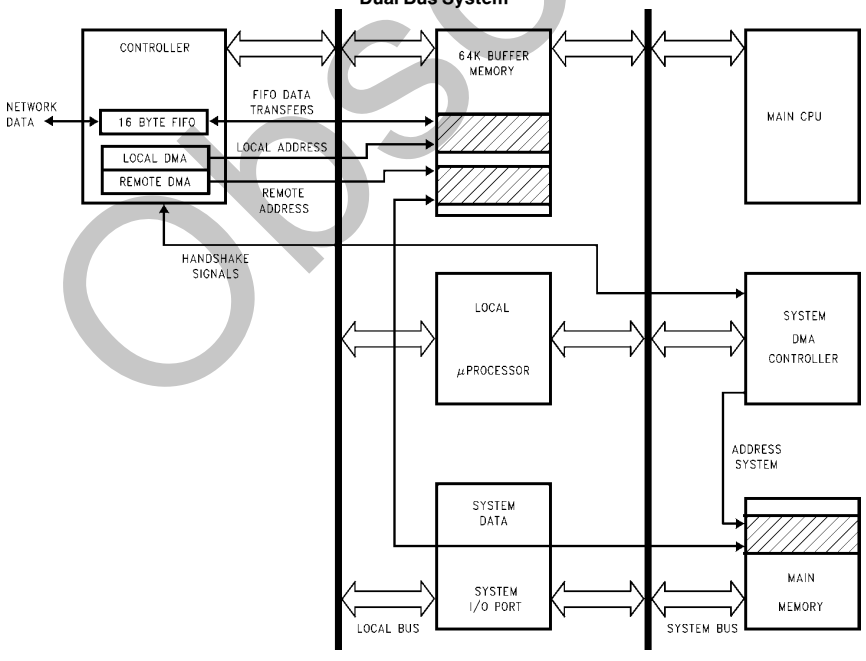
DUAL DMA CONFIGURATION

An example configuration using both the local and remote DMA channels is shown below. Network activity is isolated on a local bus, where the ST-NIC's local DMA channel performs burst transfers between the buffer memory and the ST-NIC's FIFO. The Remote DMA transfers data between the buffer memory and the host memory via a bidirectional I/O port. The Remote DMA provides local addressing capability and is used as a slave DMA by the host. Host side addressing must be provided by a host DMA or the CPU. The ST-NIC allows Local and Remote DMA operations to be interleaved.

SINGLE CHANNEL DMA OPERATION

If desirable, the two DMA channels can be combined to provide a 32-bit DMA address. The upper 16 bits of the 32-bit address are static and are used to point to a 64 kbyte (or 32k word) page of memory where packets are to be received and transmitted.

Dual Bus System



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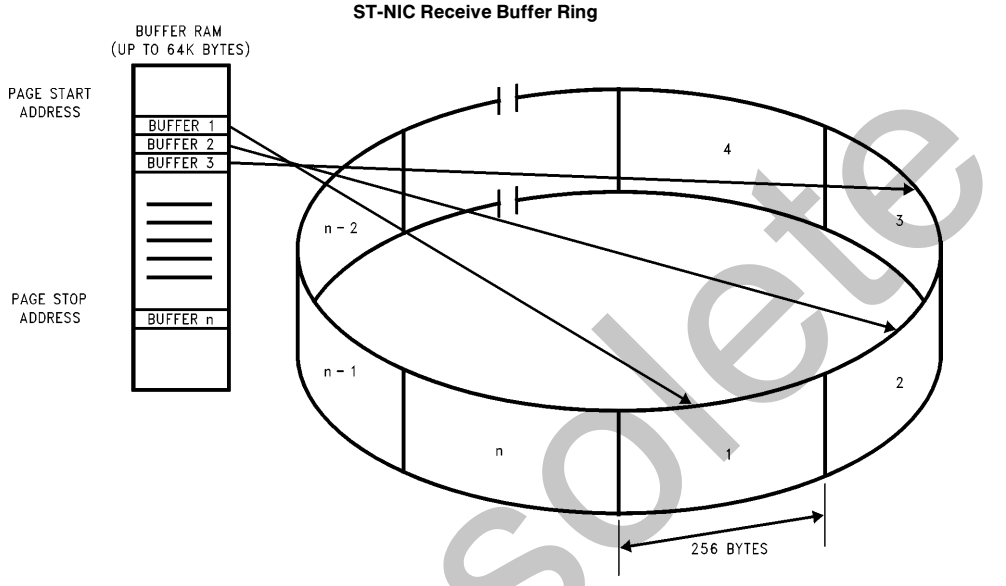
Obsolete

7.0 Packet Reception

The Local DMA receive channel uses a Buffer Ring Structure comprised of a series of contiguous fixed length 256-byte (128 word) buffers for storage of received packets. The location of the Receive Buffer Ring is programmed in two registers, a Page Start and a Page Stop Register. Ethernet packets consist of a distribution of shorter link control packets and longer data packets, the 256-byte buffer length provides a good compromise between short packets and longer packets to most efficiently use memory. In addition these buffers provide memory resources for storage of back-to-back packets in loaded networks. The assignment of buffers for storing packets is controlled by Buffer Management Logic in the ST-NIC. The Buffer Management Logic provides three basic functions: linking receive buffers for long packets, recovery of buffers when a packet is rejected, and recirculation of buffer pages that have been read by the host.

At initialization, a portion of the 64 kbyte (or 32k word) address space is reserved for the receive buffer ring. Two 8-bit registers, the Page Start Address Register (PSTART) and the Page Stop Address Register (PSTOP) define the physical boundaries of where the buffers reside. The ST-NIC treats the list of buffers as a logical ring; whenever the DMA address reaches the Page Stop Address, the DMA is reset to the Page Start Address.

ST-NIC Receive Buffer Ring



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Obsolete

7.0 Packet Reception (Continued)

INITIALIZATION OF THE BUFFER RING

Two static registers and two working registers control the operation of the Buffer Ring. These are the Page Start Register, Page Stop Register (both described previously), the Current Page Register and the Boundary Pointer Register. The Current Page Register points to the first buffer used to store a packet and is used to restore the DMA for writing status to the Buffer Ring or for restoring the DMA address in the event of a Runt packet, a CRC, or Frame Alignment error. The Boundary Register points to the first packet in the Ring not yet read by the host. If the local DMA address ever reaches the Boundary, reception is aborted. The Boundary Pointer is also used to initialize the Remote DMA for removing a packet and is advanced when a packet is removed. A simple analogy to remember the function of these registers is that the Current Page Register acts as a Write Pointer and the Boundary Pointer acts as a Read Pointer.

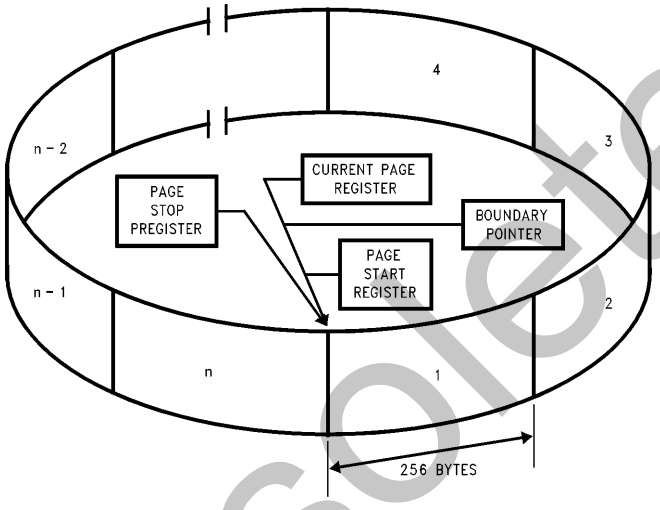
Note: At initialization, the Page Start Register value should be loaded into both Current Page Register and the Boundary Pointer Register.

Note: The Page Start Register must not be initialized to 00H.

BEGINNING OF RECEPTION

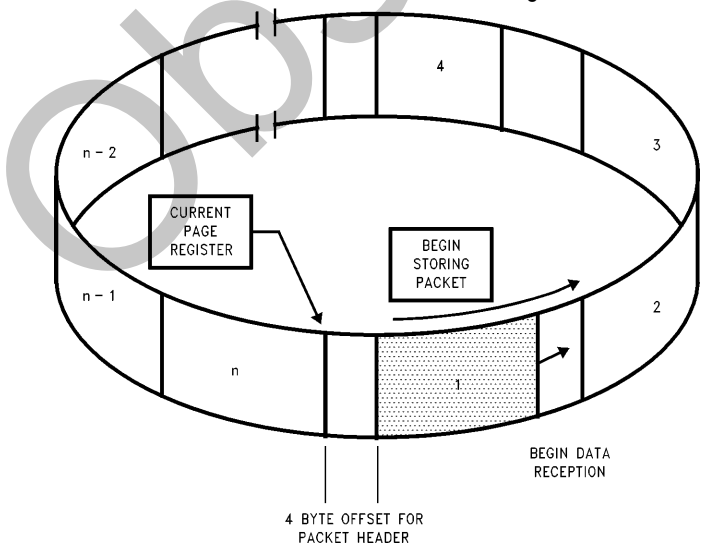
When the first packet begins arriving the ST-NIC begins storing the packet at the location pointed to by the Current Page Register. An offset of 4 bytes is saved in this first buffer to allow room for storing receive status corresponding to this packet.

Buffer Ring at Initialization



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Received Packet Enters the Buffer Pages



TL/F/11157–11

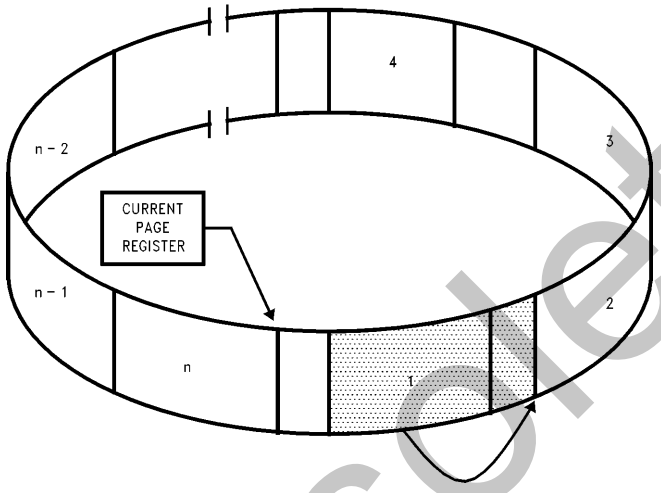
Obsolete

7.0 Packet Reception (Continued)

LINKING RECEIVE BUFFER PAGES

If the length of the packet exhausts the first 256-byte buffer, the DMA performs a forward link to the next buffer to store the remainder of the packet. For a maximum length packet the buffer logic will link six buffers to store the entire packet. Buffers cannot be skipped when linking, therefore a packet will always be stored in contiguous buffers. Before the next buffer can be linked, the Buffer Management Logic performs two comparisons. The first comparison tests for equality between the DMA address of the next buffer and the contents of the Page Stop Register. If the buffer address equals the Page Stop Register, the buffer management logic will restore the DMA to the first buffer in the Receive Buffer Ring value programmed in the Page Start Address Register. The second comparison tests for equality between the DMA address of the next buffer address and the contents of the Boundary Pointer Register. If the two values are equal the reception is aborted. The Boundary Pointer Register can be used to protect against overwriting any area in the receive buffer ring that has not yet been read. When linking buffers, buffer management will never cross this pointer, effectively avoiding any overwrites. If the buffer address does not match either the Boundary Pointer or Page Stop Address, the link to the next buffer is performed.

Linking Receive Buffer Pages



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1) Check for = to PSTOP
2) Check for = to Boundary

Obsolete

7.0 Packet Reception (Continued)

Buffer Ring Overflow

If the Buffer Ring has been filled and the DMA reaches the Boundary Pointer Address, reception of the incoming packet will be aborted by the ST-NIC. Thus, the packets previously received and still contained in the Ring will not be destroyed.

In heavily loaded network which cause overflows of the Receive Buffer Ring, the ST-NIC may disable the local DMA and suspend further receptions even if the Boundary register is advanced beyond the Current register. To guarantee this will not happen, a software reset must be issued during all Receive Buffer Ring overflows (indicated by the OVW bit in the Interrupt Status Register). The following procedure is required to recover from a Receiver Buffer Ring Overflow.

If this routine is not adhered to, the ST-NIC may act in an unpredictable manner. It should also be noted that it is not permissible to service an overflow interrupt by continuing to empty packets from the receive buffer without implementing the prescribed overflow routine. A flow chart of the ST-NIC's overflow routine follows.

Note: It is necessary to define a variable in the driver, which will be called ''Resend''.

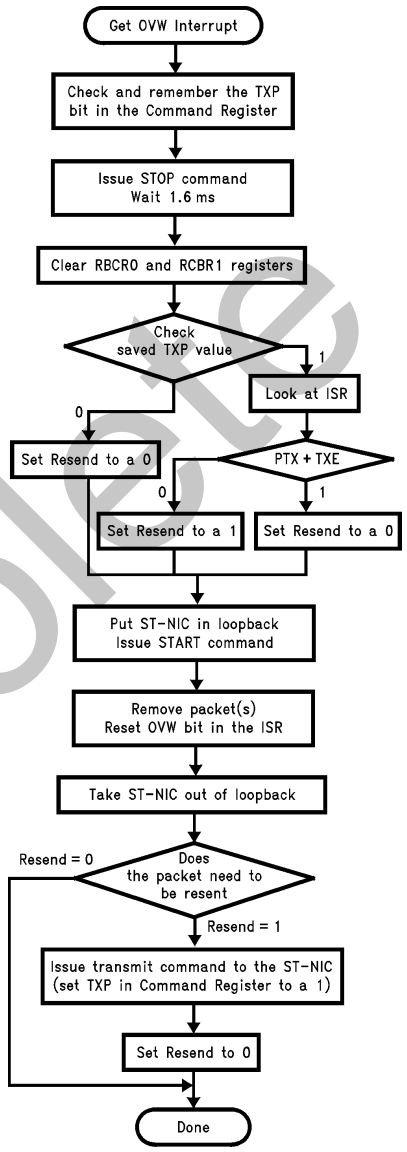
1. Read and store the value of the TXP bit in the ST-NIC Command Register.
2. Issue the STOP command to the ST-NIC. This is accomplished by setting the STP bit in the ST-NIC's Command Register. Writing 21H to the Command Register will stop the ST-NIC.
3. Wait for at least 1.6 ms. Since the ST-NIC will complete any transmission or reception that is in progress, it is necessary to time out for the maximum possible duration of an Ethernet transmission or reception. By waiting 1.6 ms this is achieved with some guard band added. Previously, it was recommended that the RST bit of the Interrupt Status Register be polled to insure that the pending transmission or reception is completed. This bit is not a reliable indicator and subsequently should be ignored.
4. Clear the ST-NIC's Remote Byte Count registers (RBCR0 and RBCR1).
5. Read the stored value of the TXP bit from step 1, above.

   If this value is a 0, set the ''Resend'' variable to a 0 and jump to step 6.

   If this value is a 1, read the ST-NIC's Interrupt Status Register. If either the Packet Transmitted bit (PTX) or Transmit Error bit (TXE) is set to a 1, set the ''Resend'' variable to a 0 and jump to step 6. If neither of these bits is set, place a 1 in the ''Resend'' variable and jump to step 6.

   This step determines if there was a transmission in progress when the stop command was issued in step 2. If there was a transmission in progress, the ST-NIC's ISR is read to determine whether or not the packet was recognized by the ST-NIC. If neither the PTX nor TXE bit was set, then the packet will essentially be lost and retransmitted only after a time-out takes place in the upper level software. By determining that the packet was lost at the driver level, a transmit command can be reissued to the ST-NIC once the overflow routine is completed (as in step 11). Also, it is possible for the ST-NIC to defer indefinitely, when it is stopped on a busy network. Step 5 also alleviates this problem. Step 5 is essential and should not be omitted from the overflow routine, in order for the ST-NIC to operate correctly.

Overflow Routine Flow Chart



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Obsolete

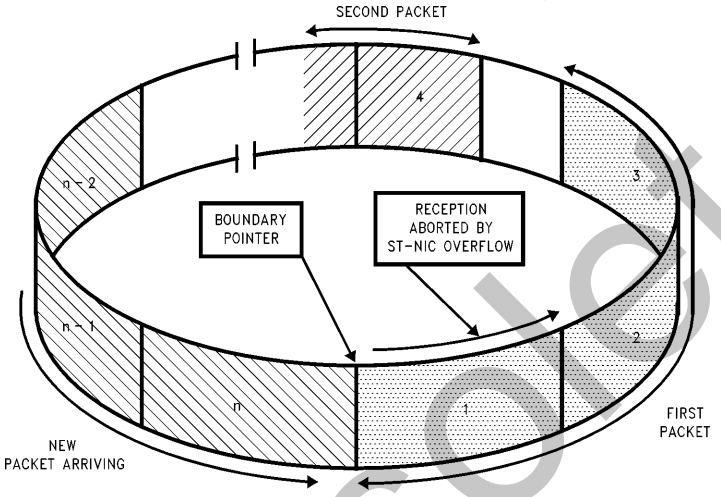
7.0 Packet Reception (Continued)

6. Place the ST-NIC in either mode 1 or mode 2 loopback. This can be accomplished by setting bits D2 and D1, of the Transmit Configuration Register, to ''0,1'' or ''1,0'', respectively.
7. Issue the START command to the ST-NIC. This can be accomplished by writing 22H to the Command Register. This is necessary to activate the ST-NIC's Remote DMA channel.
8. Remove one or more packets from the receive buffer ring.
9. Reset the overwrite warning (OVW, overflow) bit in the Interrupt Status Register.
10. Take the ST-NIC out of loopback. This is done by writing the Transmit Configration Register with the value it contains during normal operation. (Bits D2 and D1 should both be programmed to 0.)
11. If the ''Resend'' variable is set to a 1, reset the ''Resend'' variable and reissue the transmit command. This is done by writing a value of 26H to the Command Register. If the ''Resend'' variable is 0, nothing needs to be done.

Note 1: If Remote DMA is not being used, the ST-NIC does not need to be started before packets can be removed from the receive buffer ring. Hence, step 8 could be done before step 7.

Note 2: When the ST-NIC is in STOP mode, the Missed Talley Counter is disabled

Received Packet Aborted If It Hits Boundary



TL/F/11157–13

Obsolete

7.0 Packet Reception (Continued)

Enabling the ST-NIC On An Active Network

After the ST-NIC has been initialized the procedure for disabling and then re-enabling the ST-NIC on the network is similar to handling Receive Buffer Ring overflow as described previously.

1. Program Command Register for page 0 (Command Register = 21H)
2. Initialize Data Configuration Register (DCR)
3. Clear Remote Byte Count Registers (RBCR0, RBCR1)
4. Initialize Receive Configuration Register (RCR)
5. Place the ST-NIC in LOOPBACK mode 1 or 2 (Transmit Configuration Register = 02H or 04H)
6. Initialize Receive Buffer Ring: Boundary Pointer (BNDRY), Page Start (PSTART), and Page Stop (PSTOP)
7. Clear Interrupt Status Register (ISR) by writing 0FFH to it.
8. Initialize Interrupt Mask Register (IMR)
9. Program Command Register for page 1 (Command Register = 61H)
   i. Initialize Physical Address Registers (PAR0–PAR5)
   ii. Initialize Multicast Address Registers (MAR0–MAR7)
   iii. Initialize CURRent pointer
10. Put ST-NIC in START mode (Command Register = 22H). The local receive DMA is still not active since the ST-NIC is in LOOPBACK.
11. Initialize the Transmit Configuration for the intended value. The ST-NIC is now ready for transmission and reception.

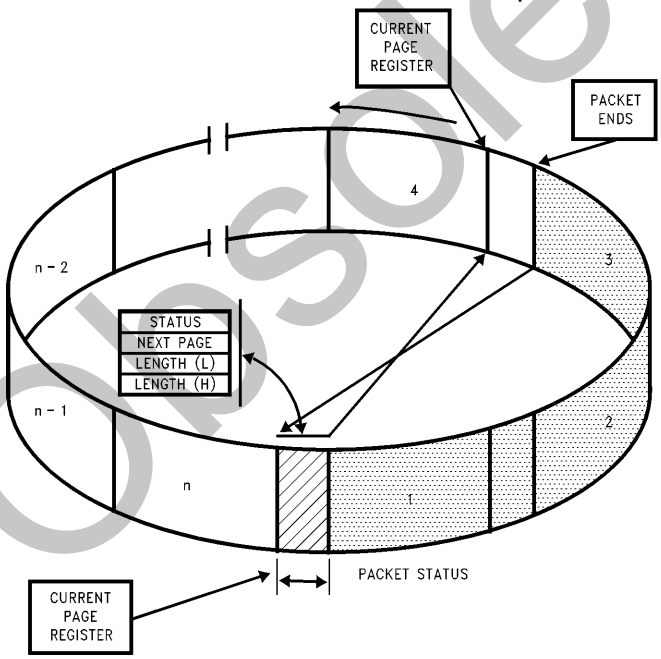
END OF PACKET OPERATIONS

At the end of the packet the ST-NIC determines whether the received packet is to be accepted or rejected. It either branches to a routine to store the Buffer Header or to another routine that recovers the buffers used to store the packet.

SUCCESSFUL RECEPTION

If the packet is successfully received, the DMA is restored to the first buffer used to store the packet (pointed to by the Current Page Register). The DMA then stores the Receive Status, a Pointer to where the next packet will be stored (Buffer 4) and the number of received bytes. Note that the remaining bytes in the last buffer are discarded and reception of the next packet begins on the next empty 256-byte buffer boundary. The Current Page Register is then initialized to the next available buffer in the Buffer Ring. (The location of the next buffer had been previously calculated and temporarily stored in an internal scratchpad register.)

Termination of Received Packet—Packet Accepted



TL/F/11157–14

Obsolete

7.0 Packet Reception (Continued)

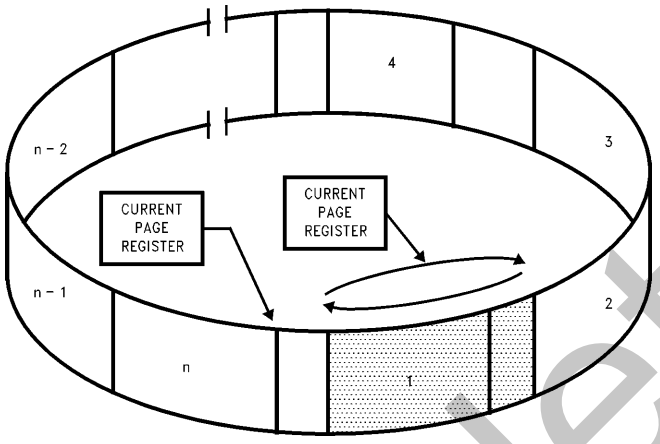
BUFFER RECOVERY FOR REJECTED PACKETS

If the packet is a runt packet or contains CRC or Frame Alignment errors, it is rejected. The buffer management logic resets the DMA back to the first buffer page used to store the packet (pointed to by CURR), recovering all buffers that had been used to store the rejected packet. This operation will not be performed if the ST-NIC is programmed to accept either runt packets or packets with CRC or Frame Alignment errors. The received CRC is always stored in buffer memory after the last byte of received data for the packet.

Error Recovery

If the packet is rejected as shown, the DMA is restored by the ST-NIC by reprogramming the DMA starting address pointed to by the Current Page Register.

Termination of Receive Packet—Packet Reject



TL/F/11157–15

Obsolete

7.0 Packet Reception (Continued)

REMOVING PACKETS FROM THE RING

Packets are removed from the ring using the Remote DMA or an external device. When using the Remote DMA the Send Packet command can be used. This programs the Remote DMA to automatically remove the received packet pointed to by the Boundary Pointer. At the end of the transfer, the ST-NIC moves the Boundary Pointer, freeing additional buffers for reception. The Boundary Pointer can also be moved manually by programming the Boundary Register.

The ST-NIC knows the difference between an empty buffer ring and a full buffer ring. This situation is seen when the Boundary Pointer (BNDRY) and the Current Page Pointer (CURR) point to the same address. If BNDRY caught up with CURR the buffer is empty and if CURR caught up with BNDRY the buffer is full.

STORAGE FORMAT FOR RECEIVED PACKETS

The following diagrams describe the format for how received packets are placed into memory by the local DMA channel. These modes are selected in the Data Configuration Register.

AD15 AD8	AD7 AD0
Next Packet Pointer	Receive Status
Receive Byte Count 1	Receive Byte Count 0
Byte 2	Byte 1

BOS = 0, WTS = 1 in Data Configuration Register. This format is used with Series 32xxx, or 680x0 processors.

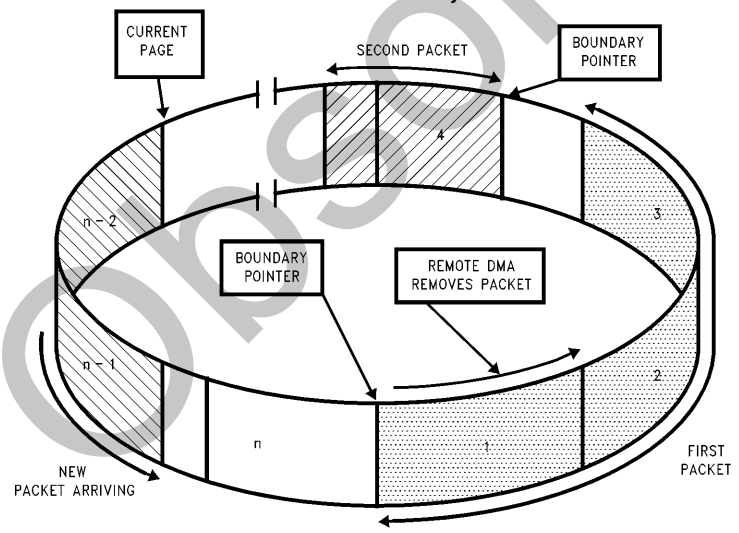
AD15 AD8	AD7 AD0
Next Packet Pointer	Receive Status
Receive Byte Count 0	Receive Byte Count 1
Byte 1	Byte 2

BOS = 1, WTS = 1 in Data Configuration Register. This format is used with 680x0 type processors. (**Note:** The Receive Count ordering remains the same for BOS = 0 or 1.)

Receive Status
Next Packet Pointer
Receive Byte Count 0
Receive Byte Count 1
Byte 0
Byte 1

BOS = 0, WTS = 0 in Data Configuration Register. This format is used with general 8-bit processors.

1st Received Packet Removed by Remote DMA



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Obsolete

8.0 Packet Transmission

The Local DMA is also used during transmission of a packet. Three registers control the DMA transfer during transmission, a Transmit Page Start Address Register (TPSR) and the Transmit Byte Count Registers (TBCR0, 1). When the ST-NIC receives a command to transmit the packet pointed to by these registers, buffer memory data will be moved into the FIFO as required during transmission. The ST-NIC will generate and append the preamble, synch and CRC fields.

General Transmit Packet Format

Transmit	Destination Address	6 Bytes
Byte	Source Address	6 Bytes
Count	Type/Length	2 Bytes
TBCR0, 1	Data Pad (If Data $<$ 46 Bytes)	$\geq$46 Bytes

TRANSMIT PACKET ASSEMBLY

The ST-NIC requires a contiguous assembled packet with the format shown. The transmit byte count includes the Destination Address, Source Address, Length Field and Data. It does not include preamble and CRC. When transmitting data smaller than 46 bytes, the packet must be padded to a minimum size of 64 bytes. The programmer is responsible for adding and stripping pad bytes.

TRANSMISSION

Prior to transmission, the TPSR (Transmit Page Start Register) and TBCR0, TBCR1 (Transmit Byte Count Registers) must be initialized. To initiate transmission of the packet the TXP bit in the Command Register is set. The Transmit Status Register (TSR) is cleared and the ST-NIC begins to prefetch transmit data from memory (unless the ST-NIC is currently receiving). If the interframe gap has timed out the ST-NIC will begin transmission.

CONDITIONS REQUIRED TO BEGIN TRANSMISSION

In order to transmit a packet, the following three conditions must be met:

1. The Interframe Gap Timer has timed out the first 6.4 μs of the Interframe Gap.
2. At least one byte has entered the FIFO. (This indicates that the burst transfer has been started.)
3. If a collision has been detected the backoff timer has expired.

In typical systems the ST-NIC prefetchs the first burst of bytes before the 6.4 μs timer expires. The time during which ST-NIC transmits preamble can also be used to load the FIFO.

Note: If carrier sense is asserted before a byte has been loaded into the FIFO, the ST-NIC will become a receiver.

COLLISION RECOVERY

During transmission, the Buffer Management logic monitors the transmit circuitry to determine if a collision has occurred. If a collision is detected, the Buffer Management logic will reset the FIFO and restore the Transmit DMA pointers for retransmission of the packet. The COL bit will be set in the TSR and the NCR (Number of Collisions Register) will be incremented. If 15 retransmissions each result in a collision the transmission will be aborted and the ABT bit in the TSR will be set.

Note: NCR reads as zeroes if excessive collisions are encountered.

TRANSMIT PACKET ASSEMBLY FORMAT

The following diagrams describe the format for how packets must be assembled prior to transmission for different byte ordering schemes. The various formats are selected in the Data Configuration Register.

D15 D8	D7 D0
Destination Address 1	Destination Address 0
Destination Address 3	Destination Address 2
Destination Address 5	Destination Address 4
Source Address 1	Source Address 0
Source Address 3	Source Address 2
Source Address 5	Source Address 4
Type/Length 1	Type/Length 0
Data 1	Data 0

BOS = 0, WTS = 1 in Data Configuration Register.

This format is used with Series 32xxx, or 808xx processors.

D15 D8	D7 D0
Destination Address 0	Destination Address 1
Destination Address 2	Destination Address 3
Destination Address 4	Destination Address 5
Source Address 0	Source Address 1
Source Address 2	Source Address 3
Source Address 4	Source Address 5
Type/Length 0	Type/Length 1
Data 0	Data 1

BOS = 1, WTS = 1 in Data Configuration Register.

This format is used with 680x0 type processors.

D1 D0
Destination Address 0
Destination Address 1
Destination Address 2
Destination Address 3
Destination Address 4
Destination Address 5
Source Address 0
Source Address 1
Source Address 2
Source Address 3
Source Address 4
Source Address 5

BOS = 0, WTS = 0 in Data Configuration Register.

This format is used with general 8-bit processors.

Note: All examples above will result in a transmission of a packet in order of DA0, DA1, DA2, DA3 . . . bits within each byte will be transmitted least significant bit first.

DA = Destination Address.

Obsolete

9.0 Remote DMA

The Remote DMA channel is used to both assemble packets for transmission, and to remove received packets from the Receive Buffer Ring. It may also be used as a general purpose slave DMA channel for moving blocks of data or commands between host memory and local buffer memory. There are three modes of operation, Remote Write, Remote Read, or Send Packet.

Two register pairs are used to control the Remote DMA, a Remote Start Address (RSAR0, RSAR1) register pair and a Remote Byte Count (RBCR0, RBCR1) register pair. The Start Address Register pair points to the beginning of the block to be moved while the Byte Count Register pair is used to indicate the number of bytes to be transferred. Full handshake logic is provided to move data between local buffer memory and a bidirectional I/O port.

REMOTE WRITE

A Remote Write transfer is used to move a block of data from the host into local buffer memory. The Remote DMA will read data from the I/O port and sequentially write it to local buffer memory beginning at the Remote Start Address. The DMA Address will be incremented and the Byte Counter will be decremented after each transfer. The DMA is terminated when the Remote Byte Count Register reaches zero.

REMOTE READ

A Remote Read transfer is used to move a block of data from local buffer memory to the host. The Remote DMA will sequentially read data from the local buffer memory, beginning at the Remote Start Address, and write data to the I/O port. The DMA Address will be incremented and the Byte Counter will be decremented after each transfer. The DMA is terminated when the Remote Byte Count Register reaches zero.

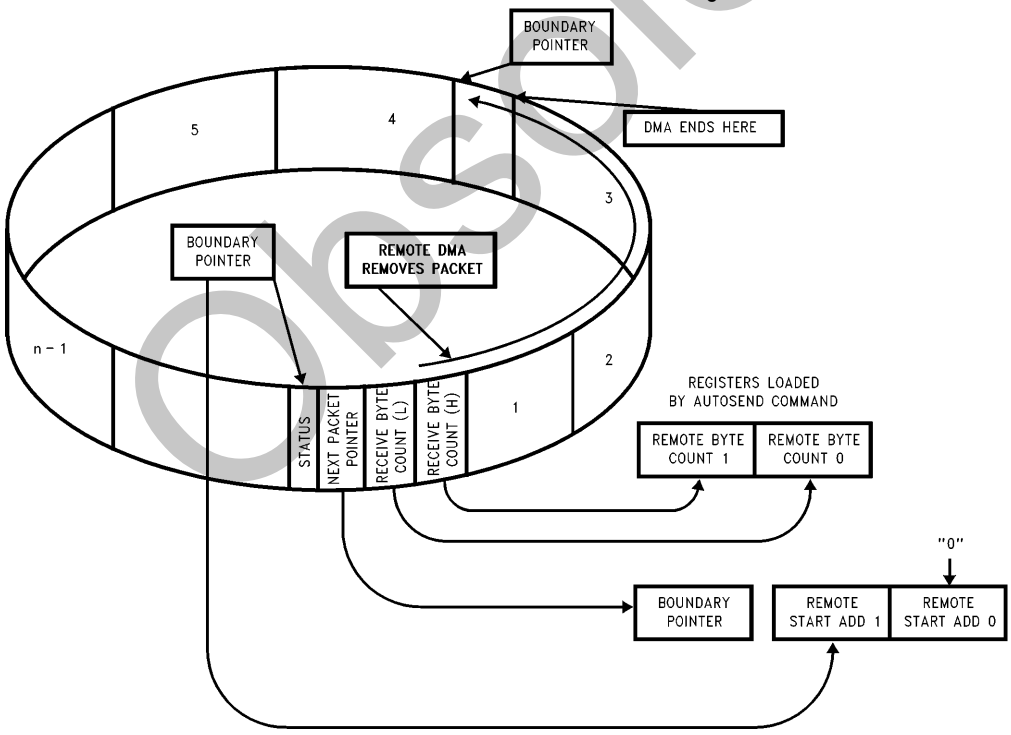
SEND PACKET COMMAND

The Remote DMA channel can be automatically initialized to transfer a single packet from the Receive Buffer Ring. The CPU begins this transfer by issuing a ''Send Packet'' Command. The DMA will be initialized to the value of the Boundary Pointer Register and the Remote Byte Count Register pair (RBCR0, RBCR1) will be initialized to the value of the Receive Byte Count fields found in the Buffer Header of each packet. After the data is transferred, the Boundary Pointer is advanced to allow the buffers to be used for new receive packets. The Remote Read will terminate when the Byte Count equals zero. The Remote DMA is then prepared to read the next packet from the Receive Buffer Ring. If the DMA pointer crosses the Page Stop Register, it is reset to the Page Start Address. This allows the Remote DMA to remove packets that have wrapped around to the top of the Receive Buffer Ring.

Note 1: In order for the ST-NIC to correctly execute the Send Packet Command, the upper Remote Byte Count Register (RBCR1) must first be loaded with 0FH.

Note 2: The Send Packet command cannot be used with 680x0 type processors.

Remote DMA Autoinitialization from Buffer Ring



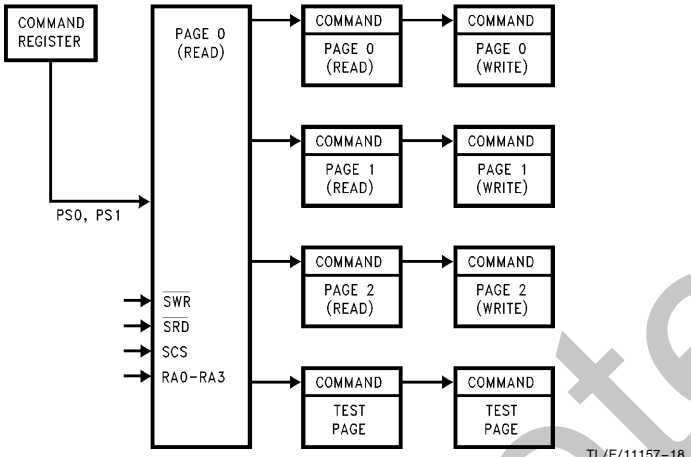
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Obsolete

10.0 Internal Registers

All registers are 8-bit wide and mapped into four pages which are selected in the Command Register (PS0, PS1). Pins RA0–RA3 are used to address registers within each page. Page 0 registers are those registers which are commonly accessed during ST-NIC operation while page 1 registers are used primarily for initialization. The registers are partitioned to avoid having to perform two write/read cycles to access commonly used registers.

10.1 REGISTER ADDRESS MAPPING



10.2 REGISTER ADDRESS ASSIGNMENTS

Page 0 Address Assignments (PS1 = 0, PS0 = 0)

RA0–RA3	RD	WR
00H	Command (CR)	Command (CR)
01H	Current Local DMA Address 0 (CLDA0)	Page Start Register (PSTART)
02H	Current Local DMA Address 1 (CLDA1)	Page Stop Register (PSTOP)
03H	Boundary Pointer (BNRY)	Boundary Pointer (BNRY)
04H	Transmit Status Register (TSR)	Transmit Page Start Address (TPSR)
05H	Number of Collisions Register (NCR)	Transmit Byte Count Register 0 (TBCR0)
06H	FIFO (FIFO)	Transmit Byte Count Register 1 (TBCR1)
07H	Interrupt Status Register (ISR)	Interrupt Status Register (ISR)
08H	Current Remote DMA Address 0 (CRDA0)	Remote Start Address Register 0 (RSAR0)
09H	Current Remote DMA Address 1 (CRDA1)	Remote Start Address Register 1 (RSAR1)
0AH	Reserved	Remote Byte Count Register 0 (RBCR0)
0BH	Reserved	Remote Byte Count Register 1 (RBCR1)
0CH	Receive Status Register (RSR)	Receive Configuration Register (RCR)
0DH	Tally Counter 0 (Frame Alignment Errors) (CNTR0)	Transmit Configuration Register (TCR)
0EH	Tally Counter 1 (CRC Errors) (CNTR1)	Data Configuration Register (DCR)
0FH	Tally Counter 2 Missed Packet Errors) (CNTR2)	Interrupt Mask Register (IMR)

Obsolete

10.0 Internal Registers (Continued)

Page 1 Address Assignments (PS1 = 0, PS0 = 1)

RA0–RA3	RD	WR
00H	Command (CR)	Command (CR)
01H	Physical Address Register 0 (PAR0)	Physical Address Register 0 (PAR0)
02H	Physical Address Register 1 (PAR1)	Physical Address Register 1 (PAR1)
03H	Physical Address Register 2 (PAR2)	Physical Address Register 2 (PAR2)
04H	Physical Address Register 3 (PAR3)	Physical Address Register 3 (PAR3)
05H	Physical Address Register 4 (PAR4)	Physical Address Register 4 (PAR4)
06H	Physical Address Register 5 (PAR5)	Physical Address Register 5 (PAR5)
07H	Current Page Register (CURR)	Current Page Register (CURR)
08H	Multicast Address Register 0 (MAR0)	Multicast Address Register 0 (MAR0)
09H	Multicast Address Register 1 (MAR1)	Multicast Address Register 1 (MAR1)
0AH	Multicast Address Register 2 (MAR2)	Multicast Address Register 2 (MAR2)
0BH	Multicast Address Register 3 (MAR3)	Multicast Address Register 3 (MAR3)
0CH	Multicast Address Register 4 (MAR4)	Multicast Address Register 4 (MAR4)
0DH	Multicast Address Register 5 (MAR5)	Multicast Address Register 5 (MAR5)
0EH	Multicast Address Register 6 (MAR6)	Multicast Address Register 6 (MAR6)
0FH	Multicast Address Register 7 (MAR7)	Multicast Address Register 7 (MAR7)

Page 2 Address Assignments (PS1 = 1, PS0 = 0)

RA0–RA3	RD	WR
00H	Command (CR)	Command (CR)
01H	Page Start Register (PSTART)	Current Local DMA Address 0 (CLDA0)
02H	Page Stop Register (PSTOP)	Current Local DMA Address 1 (CLDA1)
03H	Remote Next Packet Pointer	Remote Next Packet Pointer
04H	Transmit Page Start Address (TPSR)	Reserved
05H	Local Next Packet Pointer	Local Next Packet Pointer
06H	Address Counter (Upper)	Address Counter (Upper)
07H	Address Counter (Lower)	Address Counter (Lower)
08H	Reserved	Reserved
09H	Reserved	Reserved
0AH	Reserved	Reserved
0BH	Reserved	Reserved
0CH	Receive Configuration Register (RCR)	Reserved
0DH	Transmit Configuration Register (TCR)	Reserved
0EH	Data Configuration Register (DCR)	Reserved
0FH	Interrupt Mask Register (IMR)	Reserved

Note: Page 2 registers should only be accessed for diagnostic purposes. They should not be modified during normal operation.

Page 3 should never be modified.

Obsolete

10.0 Internal Registers (Continued)

10.3 REGISTER DESCRIPTIONS

COMMAND REGISTER (CR) 00H (READ/WRITE)

The Command Register is used to initiate transmissions, enable or disable Remote DMA operations and to select register pages. To issue a command the microprocessor sets the corresponding bit(s) (RD2, RD1, RD0, TXP). Further commands may be overlapped, but with the following rules: (1) If a transmit command overlaps with a remote DMA operation, bits RD0, RD1, and RD2 must be maintained for the remote DMA command when setting the TXP bit. Note, if a remote DMA command is re-issued when giving the transmit command, the DMA will complete immediately if the remote byte count register has not been reinitialized. (2) If a remote DMA operation overlaps a transmission, RD0, RD1, and RD2 may be written with the desired values and a ''0'' written to the TXP bit. Writing a ''0'' to this bit has no effect. (3) A remote write DMA may not overlap remote read operation or vice versa. Either of these operations must either complete or be aborted before the other operation may start. Bits PS1, PS0, RD2, and STP may be set any time.

7	6	5	4	3	2	1	0
PS1	PS0	RD2	RD1	RD0	TXP	STA	STP

Bit	Symbol	Description
D0	STP	**Stop:** Software reset command, takes the controller offline, no packets will be received or transmitted. Any reception or transmission in progress will continue to completion before entering the reset state. To exit this state, the STP bit must be reset and the STA bit must be set high. To perform a software reset, this bit should be set high. The software reset has executed only when indicated by the RST bit in the ISR being set to 1. **STP powers up high.** **Note:** If the ST-NIC has previously been in start mode and the STP is set, both the STP and STA bits will remain set.
D1	STA	**Start:** This bit is used to activate the ST-NIC after either power up, or when the ST-NIC has been placed in a reset mode by software command or error. **STA powers up low.**
D2	TXP	**Transmit Packet:** This bit must be set to initiate the transmission of a packet. TXP is internally reset either after the transmission is completed or aborted. This bit should be set only after the Transmit Byte Count and Transmit Page Start registers have been programmed.
D3, D4, and D5	RD0, RD1, and RD2	**Remote DMA Command:** These three encoded bits control operation of the Remote DMA channel. RD2 can be set to abort any Remote DMA command in progress. The Remote Byte Count Registers should be cleared when a Remote DMA has been aborted. The Remote Start Addresses are not restored to the starting address if the Remote DMA is aborted. RD2 RD1 RD0 0 0 0 Not Allowed 0 0 1 Remote Read 0 1 0 Remote Write (Note 2) 0 1 1 Send Packet 1 X X Abort/Complete Remote DMA (Note 1) **Note 1:** If a remote DMA operation is aborted and the remote byte count has not decremented to zero. PRQ will remain high. A read acknowledge (RACK) on a write acknowledge (WACK) will reset PRQ low. **Note 2:** For proper operation of the Remote Write DMA, there are two steps which must be performed before using the Remote Write DMA. The steps are as follows: I) Write a non-zero value into RBCR0. II) Set bits RD2, RD1, and RD0 to 0, 0, and 1. III) Set RBCR0, 1 and RSAR0, 1. IV) Issue the Remote Write DMA Command (RD2, RD1, RD0 = 0, 1, 0).
D6 and D7	PS0 and PS1	**Page Select:** These two encoded bits select which register page is to be accessed with addresses RA0–3. PS1 PS0 0 0 Register Page 0 0 1 Register Page 1 1 0 Register Page 2 1 1 Reserved

Obsolete

10.0 Internal Registers (Continued)

10.3 REGISTER DESCRIPTIONS (Continued)

INTERRUPT STATUS REGISTER (ISR) 07H (READ/WRITE)

This register is accessed by the host processor to determine the cause of an interrupt. Any interrupt can be masked in the Interrupt Mask Register (IMR). Individual interrupt bits are cleared by writing a ''1'' into the corresponding bit of the ISR. The INT signal is active as long as any unmasked signal is set, and will not go low until all unmasked bits in this register have been cleared. The ISR must be cleared after power up by writing it with all 1's.

7	6	5	4	3	2	1	0
RST	RDC	CNT	OVW	TXE	RXE	PTX	PRX

Bit	Symbol	Description
D0	PRX	**Packet Received:** Indicates packet received with no errors.
D1	PTX	**Packet Transmitted:** Indicates packet transmitted with no errors.
D2	RXE	**Receive Error:** Indicates that a packet was received with one or more of the following errors: — CRC Error — Frame Alignment Error — FIFO Overrun — Missed Packet
D3	TXE	**Transmit Error:** Set when packet transmitted with one or more of the following errors: — Excessive Collisions — FIFO Underrun
D4	OVW	**Overwrite Warning:** Set when receive buffer ring storage resources have been exhausted. (Local DMA has reached Boundary Pointer)
D5	CNT	**Counter Overflow:** Set when MSB of one or more of the Network Tally Counters has been set.
D6	RDC	**Remote DMA Complete:** Set when Remote DMA operation has been completed.
D7	RST	**Reset Status:** Set when ST-NIC enters reset state and cleared when a Start Command is issued to the CR. This bit is also set when a Receive Buffer Ring overflow occurs and is cleared when one or more packets have been removed from the ring. Writing to this bit has no effect. **Note:** This bit does not generate an interrupt, it is merely a status indicator.

Obsolete

10.0 Internal Registers (Continued)

10.3 REGISTER DESCRIPTIONS (Continued)

INTERRUPT MASK REGISTER (IMR) 0FH (WRITE)

The Interrupt Mask Register is used to mask interrupts. Each interrupt mask bit corresponds to a bit in the Interrupt Status Register (ISR). If an interrupt mask bit is set, an interrupt will be issued whenever the corresponding bit in the ISR is set. If any bit in the IMR is set low, an interrupt will not occur when the bit in the ISR is set. **The IMR powers up to all zeroes.**

7	6	5	4	3	2	1	0
—	RDCE	CNTE	OVWE	TXEE	RXEE	PTXE	PRXE

Bit	Symbol	Description
D0	PRXE	**Packet Received Interrupt Enable** 0: Interrupt Disabled 1: Enables Interrupt when packet received
D1	PTXE	**Packet Transmitted Interrupt Enable** 0: Interrupt Disabled 1: Enables Interrupt when packet is transmitted
D2	RXEE	**Receive Error Interrupt Enable** 0: Interrupt Disabled 1: Enables Interrupt when packet received with error
D3	TXEE	**Transmit Error Interrupt Enable** 0: Interrupt Disabled 1: Enables Interrupt when packet transmission results in error
D4	OVWE	**Overwrite Warning Interrupt Enable** 0: Interrupt Disabled 1: Enables Interrupt when Buffer Management Logic lacks sufficient buffers to store incoming packet
D5	CNTE	**Counter Overflow Interrupt Enable** 0: Interrupt Disabled 1: Enables Interrupt when MSB of one or more of the Network Statistics counters has been set
D6	RDCE	**DMA Complete Interrupt Enable** 0: Interrupt Disabled 1: Enables Interrupt when Remote DMA transfer has been completed
D7	Reserved	Reserved

Obsolete

10.0 Internal Registers (Continued)

10.3 REGISTER DESCRIPTIONS (Continued)

DATA CONFIGURATION REGISTER (DCR) 0EH (WRITE)

This Register is used to program the ST-NIC for 8- or 16-bit memory interface, select byte ordering in 16-bit applications and establish FIFO thresholds. **The DCR must be initialized prior to loading the Remote Byte Count Registers. LAS is set on power up.**

7	6	5	4	3	2	1	0
—	FT1	FT0	ARM	LS	LAS	BOS	WTS

Bit	Symbol	Description
D0	WTS	**Word Transfer Select** 0: Selects byte-wide DMA transfers 1: Selects word-wide DMA transfers ; WTS establishes byte or word transfers for both Remote and Local DMA transfers **Note:** When word-wide mode is selected up to 32k words are addressable; A0 remains low.
D1	BOS	**Byte Order Select** 0: MS byte placed on AD15–AD8 and LS byte on AD7–AD0. (32xxx, 80x86) 1: MS byte placed on AD7–AD0 and LS byte on AD15–A8. (680x0) ; Ignored when WTS is low
D2	LAS	**Long Address Select** 0: Dual 16-bit DMA mode 1: Single 32-bit DMA mode ; When LAS is high, the contents of the Remote DMA registers RSAR0, 1 are issued as A16–A31 Power up high
D3	LS	**Loopback Select** 0: Loopback mode selected. Bits D1 and D2 of the TCR must also be programmed for Loopback operation 1: Normal Operation
D4	ARM	**Auto-Initialize Remote** 0: Send Command not executed, all packets removed from Buffer Ring under program control 1: Send Command executed, Remote DMA auto-initialized to remove packets from Buffer Ring **Note:** Send Command cannot be used with 680x0 byte processors.
D5 and D6	FT0 and FT1	**FIFO Threshold Select:** Encoded FIFO threshold. Establishes point at which bus is requested when filling or emptying the FIFO. During reception, the FIFO threshold indicates the number of bytes (or words) the FIFO has filled serially from the network before bus request (BREQ) is asserted. **Note:** FIFO threshold setting determines the DMA burst length. Receive Thresholds FT1 FT0 Word Wide Byte Wide 0 0 1 Word 2 Bytes 0 1 2 Words 4 Bytes 1 0 4 Words 8 Bytes 1 1 6 Words 12 Bytes During transmission, the FIFO threshold indicates the number of bytes (or words) the FIFO has filled from the Local DMA before BREQ is asserted. Thus, the transmission threshold is 13 bytes minus the received threshold.

Obsolete

10.0 Internal Registers (Continued)

10.3 REGISTER DESCRIPTIONS (Continued)

TRANSMIT CONFIGURATION REGISTER (TCR) 0DH (WRITE)

The transmit configuration establishes the actions of the transmitter section of the ST-NIC during transmission of a packet on the network. **LB1 and LB0 which select loopback mode power up as 0.**

7	6	5	4	3	2	1	0
—	—	—	OFST	ATD	LB1	LB0	CRC

Bit	Symbol	Description
D0	CRC	**Inhibit CRC** 0: CRC appended by transmitter 1: CRC inhibited by transmitter In loopback mode CRC can be enabled or disabled to test the CRC logic
D1 and D2	LB0 and LB1	**Encoded Loopback Control:** These encoded configuration bits set the type of loopback that is to be performed. Note that loopback in mode 2 places the ENDEC Module in loopback mode and that D3 of the DCR must be set to zero for loopback operation. LB1 LB0 Mode 0 0 0 Normal Operation (LPBK = 0) Mode 1 0 1 Internal NIC Module Loopback (LPBK = 0) Mode 2 1 0 Internal ENDEC Module Loopback (LPBK = 1) Mode 3 1 1 External Loopback (LPBK = 0)
D3	ATD	**Auto Transmit Disable:** This bit allows another station to disable the ST-NIC's transmitter by transmission of a particular multicast packet. The transmitter can be re-enabled by resetting this bit or by reception of a second particular multicast packet. 1: Reception of multicast address hashing to bit 62 disables transmitter, reception of multicast address hashing to bit 63 enables transmitter.
D4	OFST	**Collision Offset Enable:** This bit modifies the backoff algorithm to allow prioritization of nodes. 0: Backoff Logic implements normal algorithm. 1: Forces Backoff algorithm modification to 0 to $2^{\min(3+n,\,10)}$ slot times for first three collisions, then follows standard backoff. (For the first three collisions, the station has higher average backoff delay making a low priority mode.)
D5	Reserved	Reserved
D6	Reserved	Reserved
D7	Reserved	Reserved

Obsolete

10.0 Internal Registers (Continued)

10.3 REGISTER DESCRIPTIONS (Continued)

TRANSMIT STATUS REGISTER (TSR) 04H (READ)

This register records events that occur on the media during transmission of a packet. It is cleared when the next transmission is initiated by the host. All bits remain low unless the event that corresponds to a particular bit occurs during transmission. Each transmission should be followed by a read of this register. The contents of this register are not specified until after the first transmission.

7	6	5	4	3	2	1	0
OWC	CDH	FU	CRS	ABT	COL	—	PTX

Bit	Symbol	Description
D0	PTX	**Packet Transmitted:** Indicates transmission without error. (No excessive collisions or FIFO underrun) (ABT = ''0'', FU = ''0'')
D1	Reserved	Reserved
D2	COL	**Transmit Collided:** Indicates that the transmission collided at least once with another station on the network. The number of collisions is recorded in the Number of Collisions Registers (NCR).
D3	ABT	**Transmit Aborted:** Indicates the ST-NIC aborted transmission because of excessive collisions. (Total number of transmissions including original transmission attempt equals 16.)
D4	CRS	**Carrier Sense Lost:** This bit is set when carrier is lost during transmission of the packet. Transmission is not aborted on loss of carrier.
D5	FU	**FIFO Underrun:** If the ST-NIC cannot gain access of the bus before the FIFO empties, this bit is set. Transmission of the packet will be aborted.
D6	CDH	**CD Heartbeat:** Failure of the transceiver to transmit a collision signal after transmission of a packet will set this bit. The Collision Detect (CD) heartbeat signal must commence during the first 6.4 μs of the Interframe Gap following a transmission. In certain collisions, the CD Heartbeat bit will be set even though the transceiver is not performing the CD heartbeat test.
D7	OWC	**Out of Window Collision:** Indicates that a collision occurred after a slot time (51.2 μs). Transmissions rescheduled as in normal collisions.

Obsolete

10.0 Internal Registers (Continued)

10.3 REGISTER DESCRIPTIONS (Continued)

RECEIVE CONFIGURATION REGISTER (RCR) 0CH (WRITE)

This register determines operation of the ST-NIC during reception of a packet and is used to program what types of packets to accept.

7	6	5	4	3	2	1	0
—	—	MON	PRO	AM	AB	AR	SEP

Bit	Symbol	Description
D0	SEP	**Save Errored Packets** 0: Packets with receive errors are rejected. 1: Packets with receive errors are accepted. Receive errors are CRC and Frame Alignment errors.
D1	AR	**Accept Runt Packets:** This bit allows the receiver to accept packets that are smaller than 64 bytes. The packet must be at least 8 bytes long to be accepted as a runt. 0: Packets with fewer than 64 bytes rejected. 1: Packets with fewer than 64 bytes accepted.
D2	AB	**Accept Broadcast:** Enables the receiver to accept a packet with an all 1's destination address. 0: Packets with broadcast destination address rejected. 1: Packets with broadcast destination address accepted.
D3	AM	**Accept Multicast:** Enables the receiver to accept a packet with a multicast address. All multicast addresses must pass the hashing array. 0: Packets with multicast destination address not checked. 1: Packets with multicast destination address checked.
D4	PRO	**Promiscuous Physical:** Enables the receiver to accept all packets with a physical address. 0: Physical address of node must match the station address programmed in PAR0–PAR5. 1: All packets with physical addresses accepted.
D5	MON	**Monitor Mode:** Enables the receiver to check addresses and CRC on incoming packets without buffering to memory. The Missed Packet Tally counter will be incremented for each recognized packet. 0: Packets buffered to memory. 1: Packets checked for address match, good CRC and Frame Alignment but not buffered to memory.
D6	Reserved	Reserved
D7	Reserved	Reserved

Note: D2 and D3 are "OR'd" together, i.e., if D2 and D3 are set the ST-NIC will accept broadcast and multicast addresses as well as its own physical address. To establish full promiscuous mode, bits D2, D3, and D4 should be set. In addition the multicast hashing array must be set to all 1's in order to accept all multicast addresses.

Obsolete

10.0 Internal Registers (Continued)

10.3 REGISTER DESCRIPTIONS (Continued)

RECEIVE STATUS REGISTER (RSR) 0CH (READ)

This register records status of the received packet, including information on errors and the type of address match, either physical or multicast. The contents of this register are written to buffer memory by the DMA after reception of a good packet. If packets with errors are to be saved the receive status is written to memory at the head of the erroneous packet if an erroneous packet is received. If packets with errors are to be rejected the RSR will not be written to memory. The contents will be cleared when the next packet arrives. CRC errors, Frame Alignment errors and missed packets are counted internally by the ST-NIC which relinguishes the Host from reading the RSR in real time to record errors for Network Management Functions. The contents of this register are not specified until after the first reception.

7	6	5	4	3	2	1	0
DFR	DIS	PHY	MPA	FO	FAE	CRC	PRX

Bit	Symbol	Description
D0	PRX	**Packet Received Intact:** Indicates packet received without error. (Bits CRC, FAE, FO, and MPA are zero for the received packet.)
D1	CRC	**CRC Error:** Indicates packet received with CRC error. Increments Tally Counter (CNTR1). This bit will also be set for Frame Alignment errors.
D2	FAE	**Frame Alignment Error:** Indicates that the incoming packet did not end on a byte boundary and the CRC did not match at the last byte boundary. Increments Tally Counter (CNTR0).
D3	FO	**FIFO Overrun:** This bit is set when the FIFO is not serviced causing overflow during reception. Reception of the packet will be aborted.
D4	MPA	**Missed Packet:** Set when a packet intended for node cannot be accepted by ST-NIC because of a lack of receive buffers or if the controller is in monitor mode and did not buffer the packet to memory. Increments Tally Counter (CNTR2).
D5	PHY	**Physical/Multicast Address:** Indicates whether received packet had a physical or multicast address type. 0: Physical Address Match 1: Multicast/Physical Address Match
D6	DIS	**Receiver Disabled:** Set when receiver disabled by entering Monitor mode. Reset when receiver is re-enabled when exiting Monitor mode.
D7	DFR	**Deferring:** Set when internal Carrier Sense or Collision signals are generated in the ENDEC module. If the transceiver has asserted the CD line as a result of the jabber, this bit will stay set indicating the jabber condition.

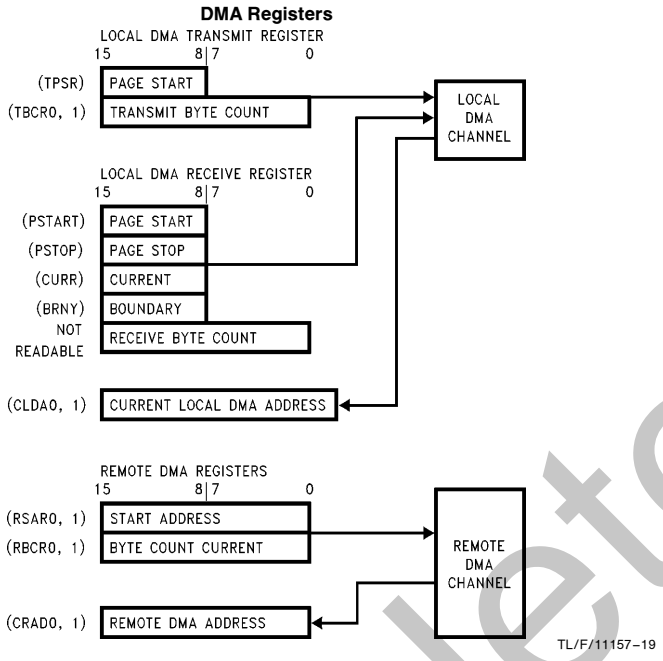
Note: Following coding applies to CRC and FAE bits.

FAE	CRC	Type of Error
0	0	No Error (Good CRC and $<$6 Dribble Bits)
0	1	CRC Error
1	0	Illegal, Will Not Occur
1	1	Frame Alignment Error and CRC Error

Obsolete

10.0 Internal Registers (Continued)

10.4 DMA REGISTERS



The DMA Registers are partitioned into groups; Transmit, Receive and Remote DMA Registers. The Transmit registers are used to initialize the Local DMA Channel for transmission of packets while the Receive Registers are used to initialize the Local DMA Channel for packet Reception. The Page Stop, Page Start, Current and Boundary Registers are used by the Buffer Management Logic to supervise the Receive Buffer Ring. The Remote DMA Registers are used to initialize the Remote DMA.

Note: In the figure above, registers are shown as 8 or 16 bits wide. Although some registers are 16-bit internal registers, all registers are accessed as 8-bit registers. Thus the 16-bit Transmit Byte Count Register is broken into two 8-bit registers, TBCR0, TBCR1. Also TPSR, PSTART, PSTOP, CURR and BNRY only check or control the upper 8 bits of address information on the bus. Thus, they are shifted to positions 15–8 in the diagram above.

10.5 TRANSMIT DMA REGISTERS

TRANSMIT PAGE START REGISTER (TPSR)

This register points to the assembled packet to be transmitted. Only the eight higher order addresses are specified since all transmit packets are assembled on 256-byte page boundaries. The bit assignment is shown below. The values placed in bits D7–D0 will be used to initialize the higher order address (A8–A15) of the Local DMA for transmission. The lower order bits (A7–A0) are initialized to zero.

Bit Assignment

	7	6	5	4	3	2	1	0
TPSR	A15	A14	A13	A12	A11	A10	A9	A8

(A7–A0 Initialized to Zero)

TRANSMIT BYTE COUNT REGISTER 0, 1 (TBCR0, TBCR1)

These two registers indicate the length of the packet to be transmitted in bytes. The count must include the number of bytes in the source, destination, length and data fields. The maximum number of transmit bytes allowed is 64 Kbytes. The ST-NIC will not truncate transmissions longer than 1500 bytes. The bit assignment is shown below:

	7	6	5	4	3	2	1	0
TBCR1	L15	L14	L13	L12	L11	L10	L9	L8

	7	6	5	4	3	2	1	0
TBCR0	L7	L6	L5	L4	L3	L2	L1	L0

Obsolete

10.0 Internal Registers (Continued)

10.6 LOCAL DMA RECEIVE REGISTERS

PAGE START AND STOP REGISTERS (PSTART, PSTOP)

The Page Start and Page Stop Registers program the starting and stopping address of the Receive Buffer Ring. Since the ST-NIC uses fixed 256-byte buffers aligned on page boundaries only the upper 8 bits of the start and stop address are specified.

PSTART, PSTOP Bit Assignment

	7	6	5	4	3	2	1	0
PSTART, PSTOP	A15	A14	A13	A12	A11	A10	A9	A8

BOUNDARY (BNRY) REGISTER

This register is used to prevent overflow of the Receive Buffer Ring. Buffer management compares the contents of this register to the next buffer address when linking buffers together. If the contents of this register match the next buffer address the Local DMA operation is aborted.

	7	6	5	4	3	2	1	0
BNRY	A15	A14	A13	A12	A11	A10	A9	A8

CURRENT PAGE REGISTER (CURR)

This register is used internally by the Buffer Management Logic as a backup register for reception. CURR contains the address of the first buffer to be used for a packet reception and is used to restore DMA pointers in the event of receive errors. This register is initialized to the same value as PSTART and should not be written to again unless the controller is Reset.

	7	6	5	4	3	2	1	0
CURR	A15	A14	A13	A12	A11	A10	A9	A8

CURRENT LOCAL DMA REGISTER 0,1 (CLDA0, 1)

These two registers can be accessed to determine the current local DMA address.

	7	6	5	4	3	2	1	0
CLDA1	A15	A14	A13	A12	A11	A10	A9	A8

	7	6	5	4	3	2	1	0
CLDA0	A7	A6	A5	A4	A3	A2	A1	A0

10.7 REMOTE DMA REGISTERS

REMOTE START ADDRESS REGISTERS (RSAR0, 1)

Remote DMA operations are programmed via the Remote Start Address (RSAR0, 1) and Remote Byte Count (RBCR0, 1) registers. The Remote Start Address is used to point to the start of the block of data to be transferred and the Remote Byte Count is used to indicate the length of the block (in bytes).

	7	6	5	4	3	2	1	0
RSAR1	A15	A14	A13	A12	A11	A10	A9	A8

	7	6	5	4	3	2	1	0
RSAR0	A7	A6	A5	A4	A3	A2	A1	A0

REMOTE BYTE COUNT REGISTERS (RBCR0, 1)

	7	6	5	4	3	2	1	0
RBCR1	BC15	BC14	BC13	BC12	BC11	BC10	BC9	BC8

	7	6	5	4	3	2	1	0
RBCR0	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0

Note: RSAR0 programs the start address bits A0–A7.
RSAR1 programs the start address bits A8–A15.
Address incremented by two for word transfers, and by one for byte transfers. Byte Count decremented by two for word transfers and by one for byte transfers.
RBCR0 programs LSB byte count.
RBCR1 programs MSB byte count.

CURRENT REMOTE DMA ADDRESS (CRDA0, CRDA1)

The Current Remote DMA Registers contain the current address of the Remote DMA. The bit assignment is shown below:

	7	6	5	4	3	2	1	0
CRDA1	A15	A14	A13	A12	A11	A10	A9	A8

	7	6	5	4	3	2	1	0
CRDA0	A7	A6	A5	A4	A3	A2	A1	A0

10.8 PHYSICAL ADDRESS REGISTERS (PAR0–PAR5)

The physical address registers are used to compare the destination address of incoming packets for rejecting or accepting packets. Comparisons are performed on a byte-wide basis. The bit assignment shown below relates the sequence in PAR0–PAR5 to the bit sequence of the received packet.

	D7	D6	D5	D4	D3	D2	D1	D0
PAR0	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
PAR1	DA15	DA14	DA13	DA12	DA11	DA10	DA9	DA8
PAR2	DA23	DA22	DA21	DA20	DA19	DA18	DA17	DA16
PAR3	DA31	DA30	DA29	DA28	DA27	DA26	DA25	DA24
PAR4	DA39	DA38	DA37	DA36	DA35	DA34	DA33	DA32
PAR5	DA47	DA46	DA45	DA44	DA43	DA42	DA41	DA40

						Destination Address		Source	
P/S	DA0	DA1	DA2	DA3	. . .	DA46	DA47	SA0	. . .

Note: P/S = Preamble, Synch
DA0 = Physical/Multicast Bit

10.9 MULTICAST ADDRESS REGISTERS (MAR0–MAR7)

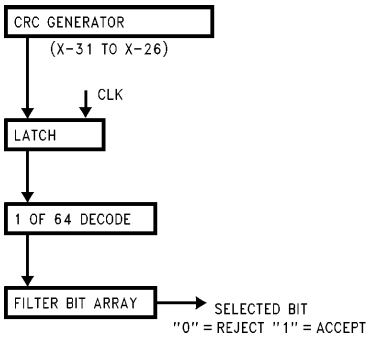
The multicast address registers provide filtering of multicast addresses hashed by the CRC logic. All destination addresses are fed through the CRC logic and as the last bit of the destination address enters the CRC, the 6 most signifi-

Obsolete

10.0 Internal Registers (Continued)

cant bits of the CRC generator are latched. These 6 bits are then decoded by a 1 of 64 decode to index a unique filter bit (FB0–63) in the multicast address registers. If the filter bit selected is set, the multicast packet is accepted. The system designer would use a program to determine which filter bits to set in the multicast registers. All multicast filter bits that correspond to multicast address accepted by the node are then set to one. To accept all multicast packets all of the registers are set to all ones.

Note: Although the hashing algorithm does not guarantee perfect filtering of multicast address, it will perfectly filter up to 64 multicast addresses if these addresses are chosen to map into unique locations in the multicast filter.



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	D7	D6	D5	D4	D3	D2	D1	D0
MAR0	FB7	FB6	FB5	FB4	FB3	FB2	FB1	FB0
MAR1	FB15	FB14	FB13	FB12	FB11	FB10	FB9	FB8
MAR2	FB23	FB22	FB21	FB20	FB19	FB18	FB17	FB16
MAR3	FB31	FB30	FB29	FB28	FB27	FB26	FB25	FB24
MAR4	FB39	FB38	FB37	FB36	FB35	FB34	FB33	FB32
MAR5	FB47	FB46	FB45	FB44	FB43	FB42	FB41	FB40
MAR6	FB55	FB54	FB53	FB52	FB51	FB50	FB49	FB48
MAR7	FB63	FB62	FB61	FB60	FB59	FB58	FB57	FB56

If address Y is found to hash to the value 32 (20H), then FB32 in MAR4 should be initialized to "1". This will cause the ST-NIC to accept any multicast packet with the address Y.

10.10 NETWORK TALLY COUNTERS

Three 8-bit counters are provided for monitoring the number of CRC errors, Frame Alignment Errors and Missed Packets. The maximum count reached by any counter is 192 (C0H). These registers will be cleared when read by the CPU. The count is recorded in binary in CT0–CT7 of each Tally Register.

Frame Alignment Error Tally (CNTR0)

This counter increments every time a packet is received with a Frame Alignment Error. The packet must have been recognized by the address recognition logic. The counter is cleared after it is read by the processor.

	7	6	5	4	3	2	1	0
CNTR0	CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0

CRC Error Tally (CNTR1)

This counter is incremented every time a packet is received with a CRC error. The packet must first be recognized by the address recognition logic. The counter is cleared after it is read by the processor.

	7	6	5	4	3	2	1	0
CNTR1	CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0

Frames Lost Tally Register (CNTR2)

This counter is incremented if a packet cannot be received due to lack of buffer resources. In monitor mode, this counter will count the number of packets that pass the address recognition logic.

	7	6	5	4	3	2	1	0
CNTR2	CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0

FIFO

This is an 8-bit register that allows the CPU to examine the contents of the FIFO after loopback. The FIFO will contain the last 8 data bytes transmitted in the loopback packet. Sequential reads from the FIFO will advance a pointer in the FIFO and allow reading of all 8 bytes.

	7	6	5	4	3	2	1	0
FIFO	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

Note: The FIFO should only be read when the ST-NIC has been programmed in loopback mode.

NUMBER OF COLLISIONS (NCR)

This register contains the number of collisions a node experiences when attempting to transmit a packet. If no collisions are experienced during a transmission attempt, the COL bit of the TSR will not be set and the contents of NCR will be zero. If there are excessive collisions, the ABT bit in the TSR will be set and the contents of NCR will be zero. The NCR is cleared after the TXP bit in the CR is set.

	7	6	5	4	3	2	1	0
NCR	—	—	—	—	NC3	NC2	NC1	NC0

Obsolete

11.0 Initialization Procedures

The ST-NIC must be initialized prior to transmission or reception of packets from the network. Power on reset is applied to the ST-NIC's reset pin. This clears/sets the following bits:

Register	Reset Bits	Set Bits
Command Register (CR)	TXP, STA	RD2, STP
Interrupt Status (ISR)		RST
Interrupt Mask (IMR)	All Bits	
Data Control (DCR)		LAS
Transmit Config. (TCR)	LB1, LB0	

The ST-NIC remains in its reset state until a Start Command is issued. This guarantees that no packets are transmitted or received and that the ST-NIC remains a bus slave until all appropriate internal registers have been programmed. After initialization the STP bit of the command register is reset and packets may be received and transmitted.

Initialization Sequence

The following initialization procedure is mandatory.

1. Program Command Register for Page 0 (Command Register = 21H)
2. Initialize Data Configuration Register (DCR)
3. Clear Remote Byte Count Registers (RBCR0, RBCR1)
4. Initialize Receive Configuration Register (RCR)
5. Place the ST-NIC in LOOPBACK mode 1 or 2 (Transmit Configuration Register = 02H or 04H)
6. Initialize Receive Buffer Ring: Boundary Pointer (BNDRY), Page Start (PSTART), and Page Stop (PSTOP)
7. Clear Interrupt Status Register (ISR) by writing 0FFH to it.
8. Initialize Interrupt Mask Register (IMR)
9. Program Command Register for page 1 (Command Register = 61H)
   - I) Initialize Physical Address Registers (PAR0–PAR5)
   - II) Initialize Multicast Address Registers (MAR0–MAR5)
   - III) Initialize CURRent pointer
10. Put ST-NIC in START mode (Command Register = 22H).
11. Initialize the Transmit Configuration Register for the intended value. The ST-NIC is now ready for transmission and reception.

Before receiving packets, the user must specify the location of the Receive Buffer Ring. This is programmed in the Page Start and Page Stop Registers. In addition, the Boundary and Current Page Register must be initialized to the value of the Page Start Register. These registers will be modified during reception of packets.

12.0 Loopback Diagnostics

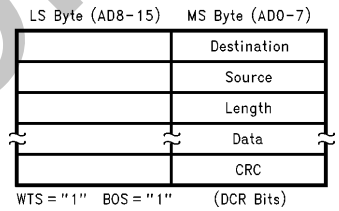
Three forms of local loopback are provided on the ST-NIC. The user has the ability to loopback through the deserializer on the controller, through the ENDEC module or the Transceiver. **Because of the half duplex architecture of the ST-NIC, loopback testing is a special mode of operation with the following restrictions:**

Restrictions During Loopback

The FIFO is split into two halves, one half is used for transmission and the other for reception. Only 8-bit fields can be fetched from memory so two tests are required for 16-bit systems to verify integrity of the entire data path. During loopback the maximum latency from the assertion of BREQ to BACK is 2.0 μs. Systems that wish to use the loopback test but do not meet this latency can limit the loopback to 7 bytes without experiencing underflow. Only the last 8 bytes of the loopback packet are retained in the FIFO. The last 8 bytes can be read through the FIFO register which will advance through the FIFO to allow reading the receive packet sequentially.

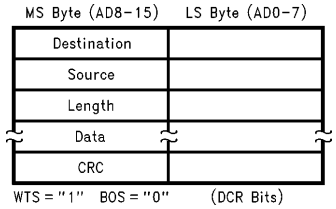
Destination Address	= (6 Bytes) Station Physical Address
Source Address	|
Length	2 Bytes
Data	= 46 to 1500 Bytes
CRC	Appended by ST-NIC if CRC = "0" in TCR

When in word-wide mode with Byte Order Select set, the loopback packet must be assembled in the even byte location as shown below. (Loopback only operates with byte wide transfers.)



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When in word-wide mode with Byte Order Select low, the following format must be used for the loopback packet.



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Note: When using loopback in word mode 2n bytes must be programmed in TBCR0, 1. Where n = actual number of bytes assembled in even or odd location.

Obsolete

12.0 Loopback Diagnostics (Continued)

To initiate a loopback the user first assembles the loopback packet then selects the type of loopback using the Transmit Configuration register bits LB0, LB1. The transmit configuration register must also be set to enable or disable CRC generation during transmission. The user then issues a normal transmit command to send the packet. During loopback the receiver checks for an address match and if CRC bit in the TCR is set, the receiver will also check the CRC. The last 8 bytes of the loopback packet are buffered and can read out of the FIFO using the FIFO read port.

Loopback Modes

MODE 1: Loopback through the NIC Module (LB1 = 0, LB0 = 1): If this loopback is used, the NIC Modules's serializer is connected to the deserializer.

MODE 2: Loopback through the ENDEC Module (LB1 = 1, LB0 = 0): If the loopback is to be performed through the SNI, the ST-NIC provides a control (LPBK) that forces the ENDEC module to loopback all signals.

MODE 3: Loopback to cable (LB1 = 1, LB0 = 1). Packets can be transmitted to the cable in loopback mode to check all of the transmit and receive paths and the cable itself.

Note: Collision and Carrier Sense can be generated by the ENDEC module and are masked by the NIC module. It is not possible to go directly between the loopback modes, it is necessary to return to normal operation (00H) when changing modes.

Reading the Loopback Packet

The last 8 bytes of a received packet can be examined by 8 consecutive reads of the FIFO register. The FIFO pointer is incremented after the rising edge of the CPU's read strobe by internally synchronizing and advancing the pointer. This may take up to four bus clock cycles, if the pointer has not been incremented by the time the CPU reads the FIFO register again, the ST-NIC will insert wait states.

Note: The FIFO may only be read during Loopback. Reading the FIFO at any other time will cause the ST-NIC to malfunction.

Alignment of the Received Packet in the FIFO

Reception of the packet in the FIFO begins at location zero, after the FIFO pointer reaches the last location in the FIFO, the pointer wraps to the top of the FIFO overwriting the previously received data. This process is continued until the last byte is received. The ST-NIC then appends the received byte count in the next two locations of the FIFO. The contents of the Upper Byte Count are also copied to the next FIFO location. The number of bytes used in the loopback packet determines the alignment of the packet in the FIFO.

The alignment for a 64-byte packet is shown below.

FIFO Location	FIFO Contents	
0	Lower Byte Count	First Byte Read
1	Upper Byte Count	Second Byte Read
2	Upper Byte Count	•
3	Last Byte	•
4	CRC1	•
5	CRC2	•
6	CRC3	•
7	CRC4	Last Byte Read

For the following alignment in the FIFO the packet length should be (N x 8) + 5 Bytes. Note that if the CRC bit in the TCR is set, CRC will not be appended by the transmitter. If the CRC is appended by the transmitter, the 1st four bytes, bytes N-3 to N, correspond to the CRC.

FIFO Location	FIFO Contents	
0	Byte N-4	First Byte Read
1	Byte N-3 (CRC1)	Second Byte Read
2	Byte N-2 (CRC2)	•
3	Byte N-1 (CRC3)	•
4	Byte N (CRC4)	•
5	Lower Byte Count	•
6	Upper Byte Count	Last Byte Read
7	Upper Byte Count	

LOOPBACK TESTS

Loopback capabilities are provided to allow certain tests to be performed to validate operation of the DP83902A ST-NIC prior to transmitting and receiving packets on a live network. Typically these tests may be performed during power up of a node. The diagnostic provides support to verify the following:

1. Verify integrity of data path. Received data is checked against transmitted data.
2. Verify the CRC logic's capability to generate good CRC on transmit, verify CRC on receive (good or bad CRC).

Obsolete

12.0 Loopback Diagnostics (Continued)

3. Verify that the Address Recognition Logic can
   a) Recognize address match packets
   b) Reject packets that fail to match an address

LOOPBACK OPERATION IN THE ST-NIC

Loopback is a modified form of transmission using only half of the FIFO. This places certain restrictions on the use of loopback testing. When loopback mode is selected in the TCR, the FIFO is split. A packet should be assembled in memory with programming of TPSR and TBCR0, TBCR1 registers. When the transmit command is issued the following operations occur:

Transmitter Actions

1. Data is transferred from memory by the DMA until the FIFO is filled. For each transfer TBCR0 and TBCR1 are decremented. (Subsequent burst transfers are initiated when the number of bytes in the FIFO drops below the programmed threshold.)
2. The ST-NIC generates 56 bits of preamble followed by an 8-bit synch pattern.
3. Data transferred from FIFO to serializer.
4. If CRC = 1 in TCR, the CRC is not calculated by ST-NIC, and the last byte transmitted is the last byte from the FIFO (Allows software CRC to be appended). If CRC = 0, ST-NIC calculates and appends four bytes of CRC.
5. At end of Transmission PTX bit set in ISR.

Receiver Actions

1. Wait for synch, all preamble stripped.
2. Store packet in FIFO, increment receive byte count for each incoming byte.
3. If CRC = 1 in TCR, receiver checks incoming packet for CRC errors. If CRC = 0 in TCR, receiver does not check CRC errors, CRC error bit always set in RSR (for address matching packets).
4. At the end of receive, the receive byte count is written into the FIFO, and the receive status register is updated. The PRX bit is typically set in the RSR even if the address does not match. If CRC errors are forced, the packet must match the address filters in order for the CRC error bit in the RSR to be set.

EXAMPLES

The following examples show what results can be expected from a properly operating ST-NIC during loopback. The restrictions and results of each type of loopback are listed for reference. The loopback tests are divided into two sets of tests. One to verify the data path, CRC generation and byte count through all three paths. The second set of tests uses internal loopback to verify the receiver's CRC checking and address recognition. For all of the tests the DCR was programmed to 40H.

Path	TCR	RCR	TSR	RSR	ISR
ST-NIC Internal	02	1F	53 (Note 1)	02 (Note 2)	02 (Note 3)

Note 1: Since carrier sense and collision detect are generated in the ENDEC module, they are blocked during NIC loopback. Carrier and CD heartbeat are not seen and the CRS and CDH bits are set.

Note 2: CRC errors are always indicated by the receiver if CRC is appended by the transmitter.

Note 3: Only the PTX bit in the ISR is set, the PRX bit is only set if status is written to memory. In loopback this action does not occur and the PRX bit remains 0 for all loopback modes.

Note 4: All values are hex.

Path	TCR	RCR	TSR	RSR	ISR
ST-NIC Internal	04	1F	43 (Note 1)	02	02

Note 1: CDH is set, CRS is not set since it is generated by the external encoder/decoder.

Path	TCR	RCR	TSR	RSR	ISR
ST-NIC External	06	1F	03 (Note 1)	02	02 (Note 2)

Note 1: CDH and CRS should not be set. The TSR however, could also contain 01H, 03H, 07H and a variety of other values depending on whether collisions were encountered or the packet was deferred.

Note 2: The ISR will contain 08H if packet is not transmittable.

Note 3: During external loopback the ST-NIC is now exposed to network traffic. It is therefore possible for the contents of both the Receive portion of the FIFO and the RSR to be corrupted by any other packet on the network. Thus in a live network the contents of the FIFO and RSR should not be depended on. The ST-NIC will still abide by the standard CSMA/CD protocol in external loopback mode. (i.e., The network will not be disturbed by the loopback packet.)

Note 4: All values are hex.

CRC AND ADDRESS RECOGNITION

The next three tests exercise the address recognition logic and CRC. These tests should be performed using internal loopback only so that the ST-NIC is isolated from interference from the network. These tests also require the capability to generate CRC in software.

The address recognition logic cannot be directly tested. The CRC and FAE bits in the RSR are only set if the address in the packet matches the address filters. If errors are expected to be set and they are not set, the packet has been rejected on the basis of an address mismatch. The following sequence of packets will test the address recognition logic. The DCR should be set to 40H and the TCR should be set to 03H with a software generated CRC.

Packet Contents			Results
Test	Address	CRC	RSR
Test A	Matching	Good	01 (Note 1)
Test B	Matching	Bad	02 (Note 2)
Test C	Non-Matching	Bad	01

Note 1: Status will read 21H if multicast address used.

Note 2: Status will read 22H if multicast address used.

Note 3: In test A, the RSR is set up. In test B the address is found to match since the CRC is flagged as bad. Test C proves that the address recognition logic can distinguish a bad address and does not notify the RSR of the bad CRC. The receiving CRC is proven to work in test A and test B.

Note 4: All values are hex.

NETWORK MANAGEMENT FUNCTIONS

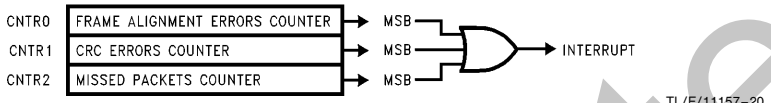
Network management capabilities are required for maintenance and planning of a local area network. The ST-NIC supports the minimum requirement for network management in hardware, the remaining requirements can be met with software counts. There are three events that software alone can not track during reception of packets: CRC errors, Frame Alignment errors, and missed packets.

Obsolete

12.0 Loopback Diagnostics (Continued)

Since errored packets can be rejected, the status associated with these packets is lost unless the CPU can access the Receive Status Register before the next packer arrives. In situations where another packet arrives very quickly, the CPU may have no opportunity to do this. The ST-NIC counts the number of packets with CRC errors and Frame Alignment errors. 8-Bit counters have been selected to reduce overhead. The counters will generate interrupts whenever their MSBs are set so that a software routine can accumulate the network statistics and reset the counter before overflow occurs. The counters are sticky so that when they reach a count of 192 (C0H) counting is halted. An additional counter is provided to count the number of packets the ST-NIC misses due to buffer overflow or being offline.

The structure of the counters is shown below:



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Additional information required for network management is available in the Receive and Transmit Status Registers. Transmit status is available after each transmission for information regarding events during transmission.

Typically, the following statistics might be gathered in software:

Traffic: Frames Sent OK
Frames Received OK
Multicast Frames Received
Packets Lost Due to Lack of Resources
Retries/Packet

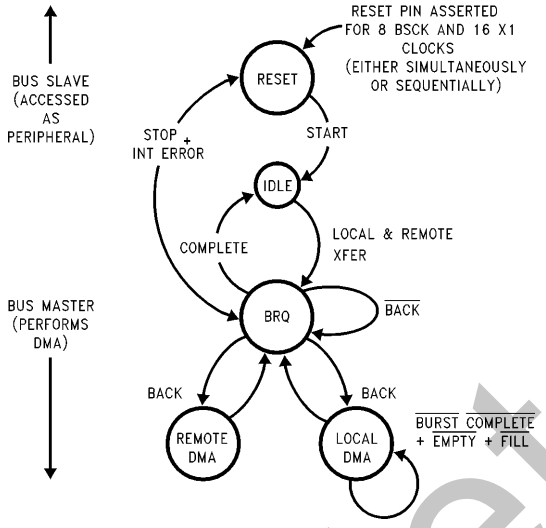
Errors: CRC Errors
Alignment Errors
Excessive Collisions
Packet with Length Errors
Heartbeat Failure

Obsolete

13.0 Bus Arbitration and Timing

The ST-NIC operates in three possible modes:

- BUS MASTER (WHILE PERFORMING DMA)
- BUS SLAVE (WHILE BEING ACCESSED BY CPU)
- IDLE



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Upon power-up the ST-NIC is in an indeterminate state. After receiving a hardware reset the ST-NIC is a bus slave in the Reset State, the receiver and transmitter are both disabled in this state. The reset state can be re-entered under three conditions, soft reset (Stop Command), hard reset (RESET input) or an error that shuts down the receiver of transmitter (FIFO underflow or overflow). After initialization of registers, the ST-NIC is issued a Start command and the ST-NIC enters Idle state. Until the DMA is required the ST-NIC remains in idle state. The idle state is exited by a request from the FIFO on the case of receiver or transmit, or from the Remote DMA in the case of Remote DMA operation. After acquiring the bus in a BREQ/BACK handshake the Remote or Local DMA transfer is completed and the ST-NIC re-enters the idle state.

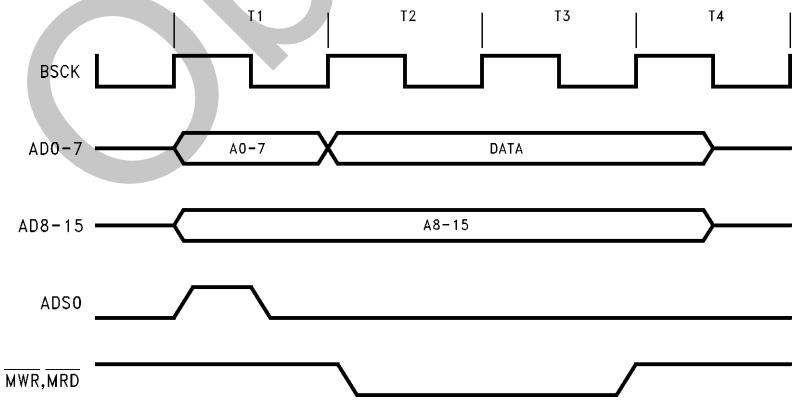
DMA TRANSFERS TIMING

The DMA can be programmed for the following types of transfers:

16-Bit Address, 8-bit Data Transfer
16-Bit Address, 16-bit Data Transfer
32-Bit Address, 8-bit Data Transfer
32-Bit Address, 16-bit Data Transfer

All DMA transfers use BSCK for timing. 16-Bit Address modes require 4 BSCK cycles as shown below:

16-Bit Address, 8-Bit Data

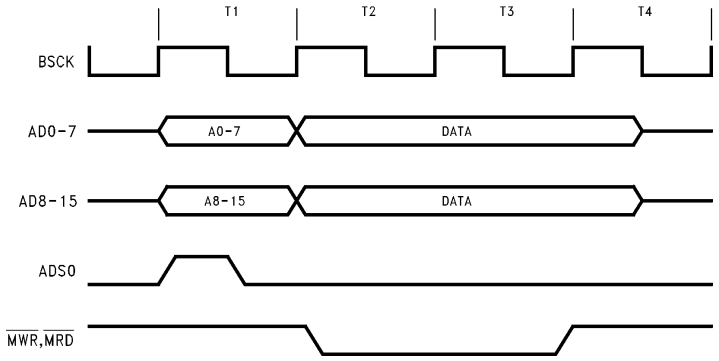


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Obsolete

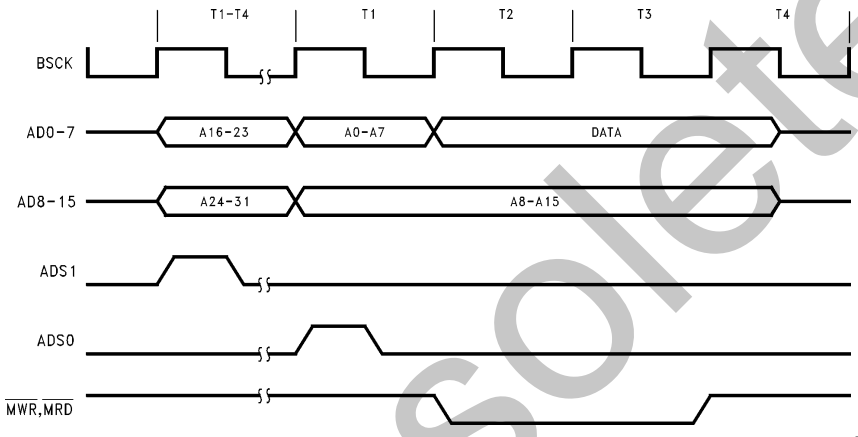
13.0 Bus Arbitration and Timing (Continued)

16-Bit Address, 16-Bit Data



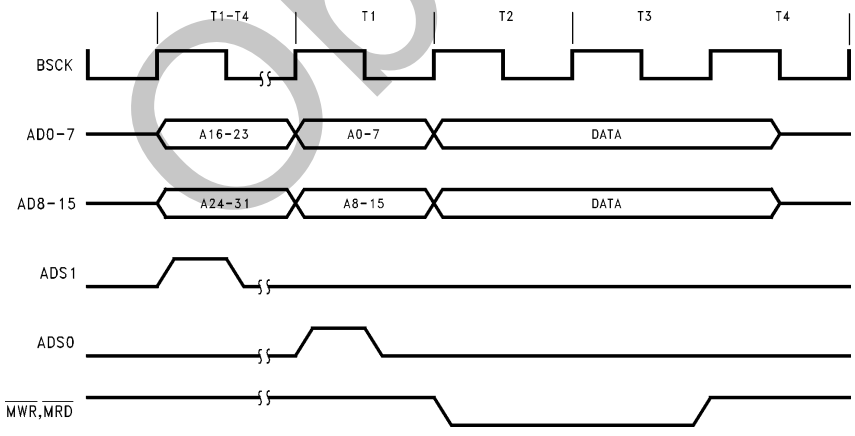
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32-Bit Address, 8-Bit Data



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32-Bit Address, 16-Bit Data



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Note: In 32-bit address mode, ADS1 is at TRI-STATE after the first T1–T4 states: thus, a 4.7k pull-down resistor is required for 32-bit address.

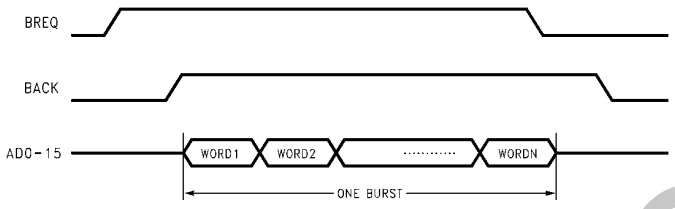
Obsolete

13.0 Bus Arbitration and Timing (Continued)

When in 32-bit mode four additional BSCK cycles are required per burst. The first bus cycle (T1′–T4′) of each burst is used to output the upper 16-bit addresses. This 16-bit address is programmed in RSAR0 and RSAR1 and points to a 64k page of system memory. All transmitted or received packets are constrained to reside within this 64k page.

FIFO BURST CONTROL

All Local DMA transfers are burst transfers, once the DMA requests the bus and the bus is acknowledged, the DMA will transfer an exact burst of bytes programmed in the Data Configuration Register (DCR) then relinquish the bus. If there are remaining bytes in the FIFO the next burst will not be initiated until the FIFO threshold is exceeded. If BACK is removed during the transfer, the burst transfer will be aborted. **(DROPPING BACK DURING A DMA CYCLE IS NOT RECOMMENDED.)**

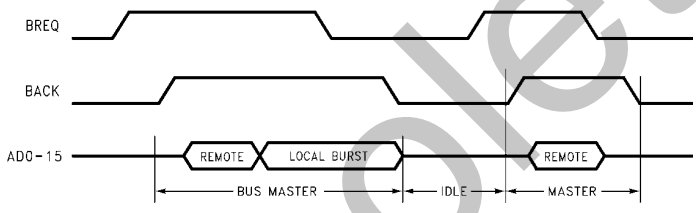


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where N = 1, 2, 4, or 6 Words or N = 2, 4, 8, or 12 Bytes when in byte mode.

INTERLEAVED LOCAL OPERATION

If a remote DMA transfer is initiated or in progress when a packet is being received or transmitted, the Remote DMA transfer will be interrupted for higher priority Local DMA transfers. When the Local DMA transfer is completed the Remote DMA will rearbitrate for the bus and continue its transfers. This is illustrated below:



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Note that if the FIFO requires service while a remote DMA is in progress, BREQ is not dropped and the Local DMA burst is appended to the Remote Transfer. When switching from a local transfer to a remote transfer, however, BREQ is dropped and raised again. This allows the CPU or other devices to fairly contend for the bus.

FIFO AND BUS OPERATIONS

Overview

To accommodate the different rates at which data comes from (or goes to) the network and goes to (or comes from) the system memory, the ST-NIC contains a 16-byte FIFO for buffering data between the bus and the media. The FIFO threshold is programmable, allowing filling (or emptying) the FIFO at different rates. When the FIFO has filled to its programmed threshold, the local DMA channel transfers these bytes (or words) into local memory. It is crucial that the local DMA is given access to the bus within a minimum bus latency time; otherwise a FIFO underrun (or overrun) occurs.

To understand FIFO underruns or overruns, there are two causes which produce this condition—

1. the bus latency is so long that the FIFO has filled (or emptied) from the network before the local DMA has serviced the FIFO.
2. the bus latency or bus data rate has slowed the throughput of the local DMA to a point where it is slower than the network data rate (10 Mb/s). This second condition is also dependent upon DMA clock and word width (byte wide or word wide).

The worst case condition ultimately limits the overall bus latency which the ST-NIC can tolerate.

FIFO Underrun and Transmit Enable

During transmission, if a FIFO underrun occurs, the Transmit enable (TXE) output may remain high (active). Generally, this will cause a very large packet to be transmitted onto the network. The jabber feature of the transceiver will terminate the transmission, and reset TXE.

To prevent this problem, a properly designed system will not allow FIFO underruns by giving the ST-NIC a bus acknowledge within time shown in the maximum bus latency curves shown and described later.

FIFO at the Beginning of Receive

At the beginning of reception, the ST-NIC stores entire Address field of each incoming packet in the FIFO to deter-

Obsolete

13.0 Bus Arbitration and Timing (Continued)

mine whether the packet matches its Physical Address Registers or maps to one of its Multicast Registers. This causes the FIFO to accumulate 8 bytes. Furthermore, there are some synchronization delays in the DMA PLA. Thus, the actual time that BREQ is asserted from the time the Start of Frame Delimiter (SFD) is detected is 7.8 μs. This operation affects the bus latencies at 2- and 4-byte thresholds during the first receive BREQ since the FIFO must be filled to 8 bytes (or 4 words) before issuing a BREQ.

FIFO Operation at the End of Receive

When Carrier Sense goes low, the ST-NIC enters its end of packet processing sequence, emptying its FIFO and writing the status information at the beginning of the packet, *Figure 5*. The ST-NIC holds onto the bus for the entire sequence. The longest time BREQ may be extended occurs when a packet ends just as the ST-NIC performs its last FIFO burst. The ST-NIC, in this case, performs a programmed burst transfer followed by flushing the remaining bytes in the FIFO, and completes by writing the header information to memory. The following steps occur during this sequence.

1. ST-NIC issues BREQ because the FIFO threshold has been reached
2. During the burst, packet ends, resulting in BREQ extended.
3. ST-NIC flushes remaining bytes from FIFO
4. ST-NIC performs internal processing to prepare for writing the header.
5. ST-NIC writes 4-byte (2-word) header
6. ST-NIC deasserts BREQ

End of Packet Processing (EOPP) times for 10 MHz and 20 MHz have been tabulated in the table below.

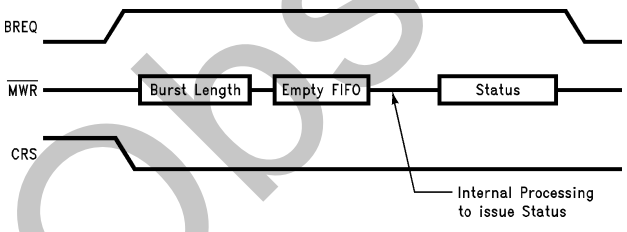
Mode	Threshold	Bus Clock	EOPP
Byte	2 Bytes	10 MHz	7.0 μs
	4 Bytes		8.6 μs
	8 Bytes		11.0 μs
Byte	2 Bytes	20 MHz	3.6 μs
	4 Bytes		4.2 μs
	8 Bytes		5.0 μs
Word	2 Bytes	10 MHz	5.4 μs
	4 Bytes		6.2 μs
	8 Bytes		7.4 μs
Word	2 Bytes	20 MHz	3.0 μs
	4 Bytes		3.2 μs
	8 Bytes		3.6 μs

End of Packet Processing Times for Various FIFO Thresholds, Bus Clocks and Transfer Modes

Threshold Detection (Bus Latency)

To assure that no overwriting of data in the FIFO occurs, the FIFO logic flags a FIFO overrun as the 13th byte is written into the FIFO, effectively shortening the FIFO to 13 bytes. The FIFO logic also operates differently in Byte Mode and in Word Mode. In Byte Mode, a threshold is indicated when the n+1 byte has entered the FIFO; thus, with an 8-byte threshold, the ST-NIC issues Bus Request (BREQ) when the 9th byte has entered the FIFO. For Word Mode, BREQ is not generated until the n+2 bytes have entered the FIFO. Thus, with a 4-word threshold (equivalent to 8-byte threshold), BREQ is issued when the 10th byte has entered the FIFO. The two graphs, following, indicate the maximum allowable bus latency for Word and Byte transfer modes.

End of Packet Processing



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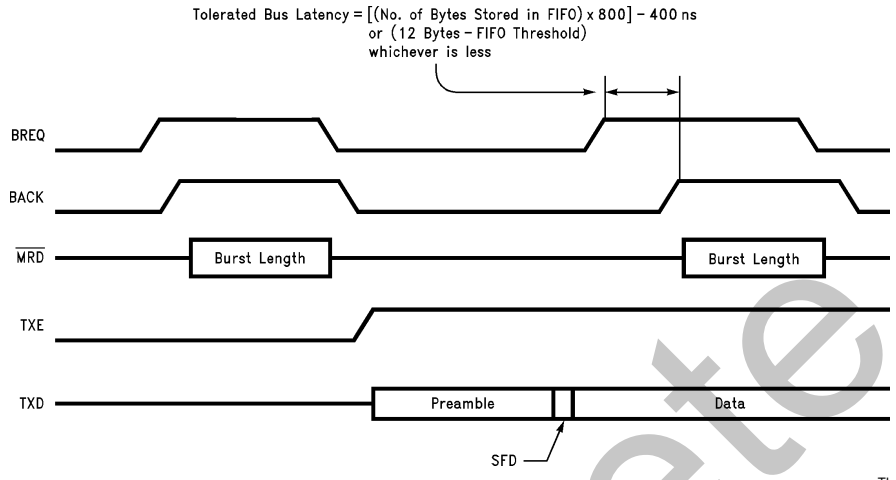
Obsolete

13.0 Bus Arbitration and Timing (Continued)

The FIFO at the Beginning of Transmit

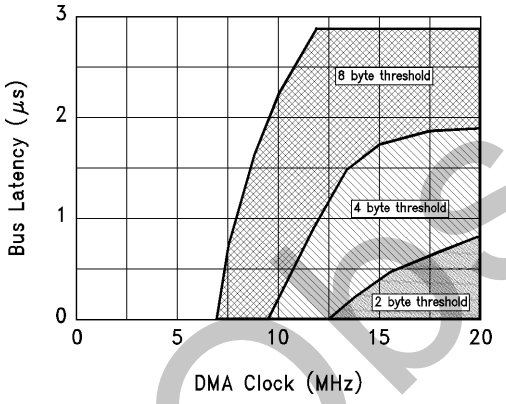
Before transmitting, the ST-NIC performs a prefetch from memory to load the FIFO. The number of bytes prefetched is the programmed FIFO threshold. The next BREQ is not issued until after the ST-NIC actually begins transmitting data, i.e., after SFD. The Transmit Prefetch diagram illustrates this process.

Transmit Prefetch Timing



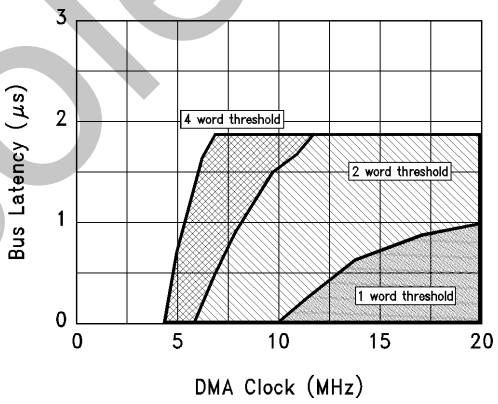
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Maximum Bus Latency for Byte Mode



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Maximum Bus Latency for Word Mode



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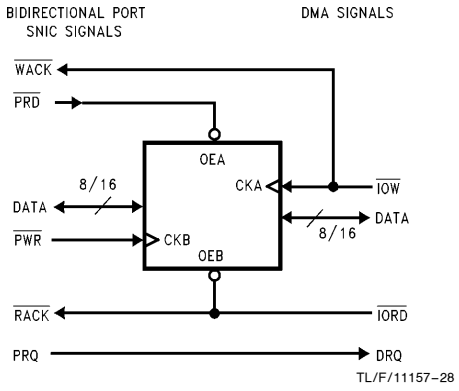
Obsolete

13.0 Bus Arbitration and Timing (Continued)

REMOTE DMA-BIDIRECTIONAL PORT CONTROL

The Remote DMA transfers data between the local buffer memory and a bidirectional port (memory to I/O transfer). This transfer is arbited on a byte by byte basis versus the burst transfer used for Local DMA transfers. This bidirectional port is also read/written by the host. All transfers through this port are asynchronous. At any one time transfers are limited to one direction, either from the port to local buffer memory (Remote Write) or from local buffer memory to the port (Remote Read).

Bus Handshake Signals for Remote DMA Transfers



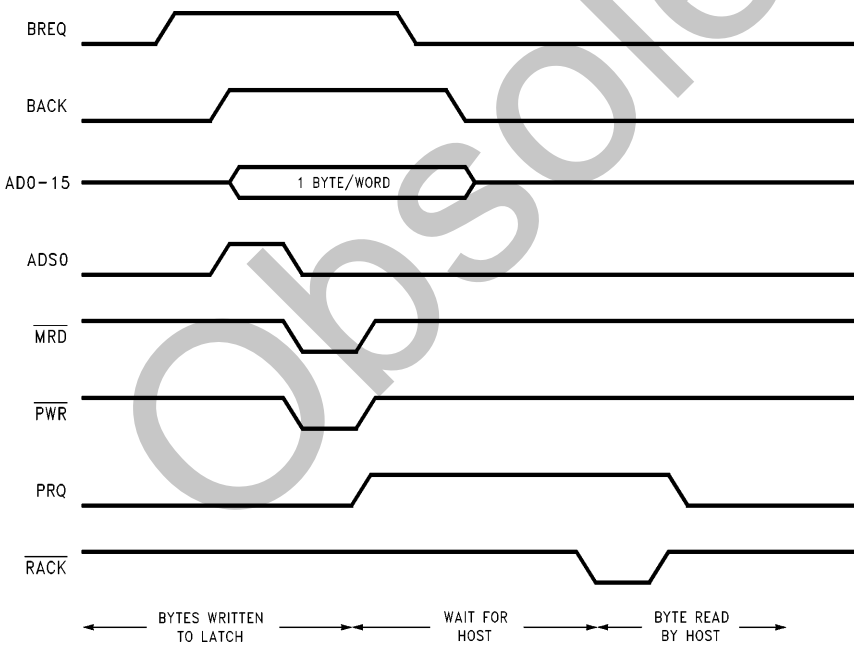
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REMOTE READ TIMING

1. The DMA reads byte/word from local buffer memory and writes byte/word into latch, increments the DMA address and decrements the byte count (RBCR0, 1).
2. A Request Line (PRQ) is asserted to inform the system that a byte is available.
3. The system reads the port, the read strobe ($\overline{RACK}$) is used as an acknowledge by the Remote DMA and it goes back to step 1.

Steps 1–3 are repeated until the remote DMA is complete.

Note that in order for the Remote DMA to transfer a byte from memory to the latch, it must arbitrate access to the local bus via a BREQ, BACK handshake. After each byte or word is transferred to the latch, BREQ is dropped. If a Local DMA is in progress, the Remote DMA is held off until the local DMA is complete.



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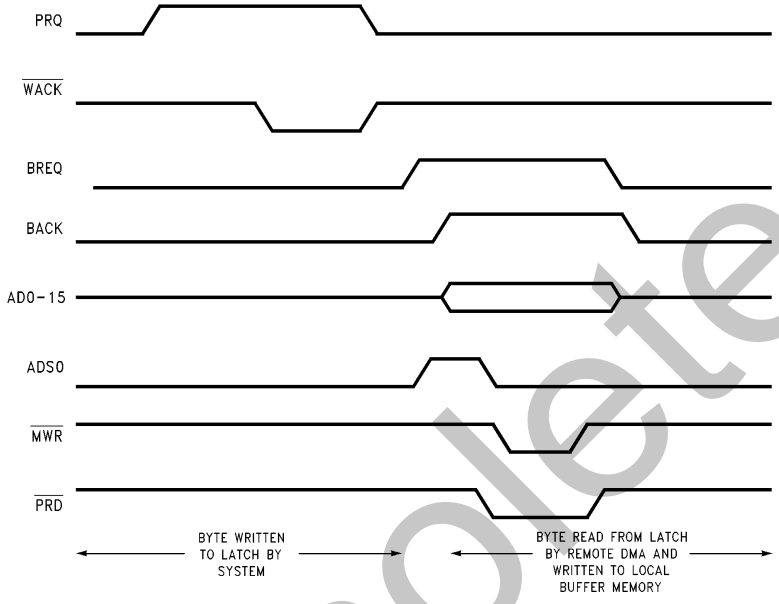
13.0 Bus Arbitration and Timing (Continued)

REMOTE WRITE TIMING

A Remote Write operation transfers data from the I/O port to the local buffer RAM. The ST-NIC initiates a transfer by requesting a byte/word via the PRQ. The system transfers a byte-word to the latch via $\overline{IOW}$. This write strobe is detected by the ST-NIC and PRQ is removed. By removing the PRQ, the Remote DMA holds off further transfers into the latch until the current byte/word has been transferred from the latch, PRQ is reasserted and the next transfer can begin.

1. ST-NIC asserts PRQ. System writes byte/word into latch. ST-NIC removes PRQ.
2. Remote DMA reads contents of port and writes byte/word to local buffer memory, increments address and decrements byte count (RBCR0, 1).
3. Go back to step 1.

   Steps 1–3 are repeated until the remote DMA is complete.



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REMOTE DMA WRITE SPECIAL CONSIDERATIONS

Setting PRQ Using the Remote Read

Under certain conditions the ST-NIC bus state machine may issue $\overline{MWR}$ and $\overline{PRD}$ before PRQ for the first DMA transfer of a Remote Write Command. If this occurs this could cause data corruption, or cause the remote DMA count to be different from the main CPU count causing the system to ''lock up''.

To prevent this condition when implementing a Remote DMA Write, the Remote DMA Write command should first be preceded by a Remote DMA Read command to insure that the PRQ signal is asserted before the ST-NIC starts its port read cycle. The reason for this is that the state machine that asserts PRQ runs independently of the state machine that controls the DMA signals. The DMA machine assumes that PRQ is asserted, but actually may not be. To remedy this situation, a single Remote Read cycle should be inserted before the actual DMA Write Command is given. This will ensure that PRQ is asserted when the Remote DMA Write is subsequently executed. This single Remote Read cycle is called a ''dummy Remote Read''. In order for the dummy Remote Read cycle to operate correctly, the Start Address should be programmed to a known, safe location in the buffer memory space, and the Remote Byte count should be programmed to a value greater than 1. This will ensure that the master read cycle is performed safely, eliminating the possibility of data corruption.

Remote Write with High Speed Buses

When implementing the Remote DMA Write solution with high speed buses and CPU's, timing may cause the system to hang. Therefore additional considerations are required.

A problem occurs when the system can execute the dummy Remote Read and then start the Remote Write before the ST-NIC has had a chance to execute the Remote Read. If this happens the PRQ signal will not get set, and the Remote Byte Count and Remote Start Address for the Remote Write operation could be corrupted. This is shown by the hatched waveforms in the following timing diagram. The execution of the Remote Read can be delayed by the local DMA operations (particularly during end-of-packet processing).

To ensure the dummy Remote Read does execute, a delay must be inserted between writing the Remote Read Command, and starting to write the Remote Write Start Address. (This time is designated in the next figure by the delay arrows.) The recommended method to avoid this problem is after the Remote Read command is given, to poll both bytes of the Current Remote DMA Address Registers. When the address has incremented PRQ has been set. Software should recognize this and then start the Remote Write.

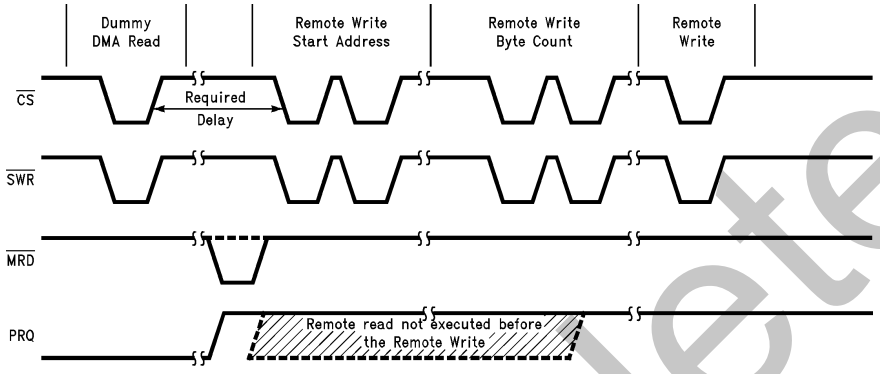
Obsolete

13.0 Bus Arbitration and Timing (Continued)

An additional caution for high speed systems is that the polling must follow guidelines specified in the Time Between Chip Selects section. That is, there must be at least 4 bus clocks between chip selects. (For example when BSCK = 20 MHz, then this time should be 200 ns).

The general flow for executing a Remote Write is:

1. Set Remote Byte Count to a value >1 and Remote Start Address to unused RAM (one location before the transmit start address is usually a safe location).
2. Issue the ''dummy'' Remote Read command.
3. Read the Current Remote DMA Address (CRDA) (both bytes).
4. Compare to previous CRDA value if different go to 6.
5. Delay and jump to 3.
6. Set up for the Remote Write command, by setting the Remote Byte Count and the Remote Start Address (note that if the Remote Byte count in step 1 can be set to the transmit byte count plus one, and the Remote Start Address to one less, these will now be incremented to the correct values.)
7. Issue the Remote Write command.



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Note: The dashed lines indicate incorrect timing as described in text.

Timing Diagram for Dummy Remote Read

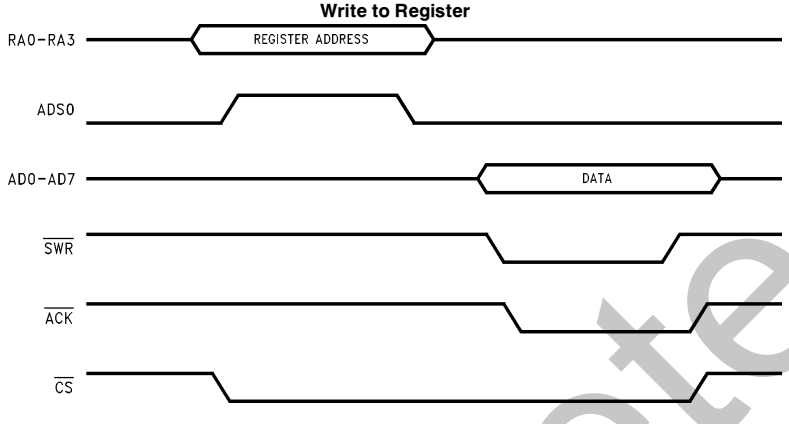
Obsolete

13.0 Bus Arbitration and Timing (Continued)

SLAVE MODE TIMING

When $\overline{CS}$ is low, the ST-NIC becomes a bus slave. The CPU can then read or write any internal registers. All register accesses are byte wide. The timing for register access is shown below. The host CPU accesses internal registers with four address lines, RA0–RA3, $\overline{SRD}$ and $\overline{SWR}$ strobes. ADS0 is used to latch the address when interfacing to a multiplexed, address data bus. Since the ST-NIC may be a local bus master when the host CPU attempts to read or write to the controller, an $\overline{ACK}$ line is used to hold off the CPU until the ST-NIC leaves master mode. Some number of BSCK cycles is also required to allow the ST-NIC to synchronize to the read or write cycles.

Write to Register



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Read from Register

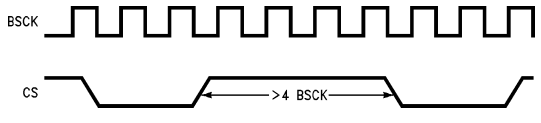


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TIME BETWEEN CHIP SELECTS

The ST-NIC requires that successive chip selects be no closer than 4 bus clocks (BSCK) together. If the condition is violated, the ST-NIC may glitch $\overline{ACK}$. CPUs that operate from pipelined instructions (i.e., 386) or have a cache (i.e., 486) can execute consecutive I/O cycles very quickly. The solution is to delay the execution of consecutive I/O cycles by either breaking the pipeline or forcing the CPU to access outside its cache.

Time between Chip Selects



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Obsolete

14.0 Preliminary Electrical Characteristics

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−0.5V to V_{CC} + 0.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} + 0.5V
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (PD)	800 mW
Lead Temp. (TL) (Soldering, 10 sec.)	260°C
ESD Rating (R_{ZAP} = 1.5k, C_{ZAP} = 100 pF)	1.5 kV
Pin to Pin	
Pin to GND	
Pin to V_{CC} (±1 ZAP)	
Clamp Diode Current	±20 mA

Note: *Absolute Maximum ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits.*

Note: *All specifications in this datasheet are valid only if the mandatory isolation is employed and all differential signals are taken to exist at the AUI or TPI side of the isolation.*

Preliminary DC Specifications T_A = 0°C to 70°C, V_{CC} = 5V ±5%, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Max	Units
V_{OH}	Minimum High Level Output Voltage (Notes 1, 4)	I_{OH} = −20 μA I_{OH} = −2.0 mA	V_{CC} −0.1 3.5		V V
V_{OL}	Minimum Low Level Output Voltage (Notes 1, 4)	I_{OL} = 20 μA I_{OL} = 2.0 mA		0.1 0.4	V V
V_{IH}	Minimum High Level Input Voltage (Note 2)		2.0		V
V_{IH2}	Minimum High Level Input Voltage For RACK WACK (Note 2)		2.7		V
V_{IL}	Maximum Low Level Input Voltage (Note 2)			0.8	V
V_{IL2}	Maximum Low Level Input Voltage For RACK, WACK (Note 2)			0.6	V
V_{LOL}	Good Link Output Voltage	I_{OL} = 16 mA		0.4	V
I_{IN}	Input Current	V_I = V_{CC} or GND	−1.0	+1.0	μA
I_{INSEL}	Input Current	V_{IN} = V_{CC} V_{IN} = GND	50 −1	2000 +1	μA μA
I_{OZ}	Minimum TRI-STATE Output Leakage Current (Note 5)	V_{OUT} = V_{CC} or GND	−10	+10	μA
I_{CC}	Average Supply Current (Note 3)	X1 = 20 MHz Clock I_{OUT} = 0 μA V_{IN} = V_{CC} or GND		140	mA

Note 1: These levels are tested dynamically using a limited amount of functional test patterns, please refer to AC test load.

Note 2: Limited functional test patterns are performed at these input levels. The majority of functional tests are performed at levels of 0V and 3V.

Note 3: This is measured with a 0.1 μF bypass capacitor between V_{CC} and GND.

Note 4: The low drive CMOS compatible V_{OH} and V_{OL} limits are not tested directly. Detailed device characterization validates that this specification can be guaranteed by testing the high drive TTL compatible V_{OL} and V_{OH} specification.

Note 5: RA0–RA3, $\overline{PRD}$, $\overline{WACK}$, BREQ and INT pins are used as outputs in test mode and as a result are tested as if they are TRI-STATE input/outputs. For these pins the input leakage specification is I_{OZ}.

Obsolete

14.0 Preliminary Electrical Characteristics (Continued)

Preliminary DC Specifications T_A = 0°C to 70°C, V_{CC} = 5V ±5%, unless otherwise specified. (Continued)

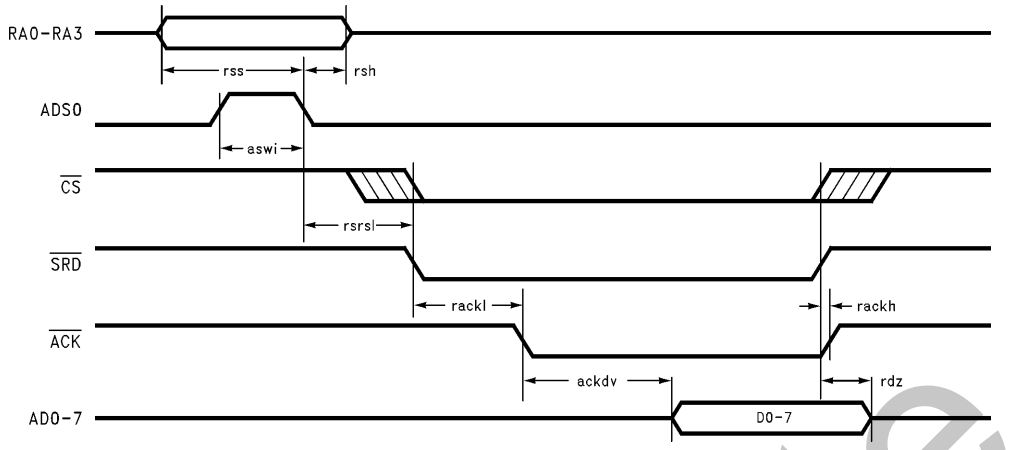
Symbol	Parameter	Conditions	Min	Max	Units
AUI INTERFACE PINS (TX±, RX±, and CD±)					
V_{OD}	Diff. Output Voltage (TX±)	78Ω Termination, and 270Ω from Each to GND	±550	±1200	mV
V_{OB}	Diff. Output Voltage Imbalance (TX±) (Note 1)	78Ω Termination, and 270Ω from Each to GND	Typical: 40 mV		
V_U	Undershoot Voltage (TX±) (Note 1)	78Ω Termination, and 270Ω from Each to GND	Typical: 80 mV		
V_{DS}	Diff. Squelch Threshold (RX± and CD±) (Note 1)		−175	−300	mV
V_{CM}	Diff. Input Common Mode Voltage (RX± and CD±) (Note 1)		0	5.25	V
OSCILLATOR PINS (X1 AND X2)					
V_{IH}	X1 Input High Voltage	X1 is Connected to an Oscillator and GND/X2 is Grounded	2.0		V
V_{IL}	X1 Input Low Voltage	X1 is Connected to an Oscillator and GND/X2 is Grounded		0.8	V
I_{OSC}	X1 Input Current	GND/X2 is Grounded V_{IN} = V_{CC} or GND		3	mA
I_{X2}	X2 Input Current	X2 Grounded (Driven Mode)		4	mA
TWISTED PAIR INTERFACE PINS (TXO±, TXOd±, and RXI±)					
R_{TOL}	TXOd±, TXO± Low Level Output Resistance	I_{OL} = 25 mA		15	Ω
R_{TOH}	TXOd±, TXO± High Level Output Resistance	I_{OH} = 25 mA		15	Ω
V_{SRON1}	Receive Threshold Turn-On Voltage (10BASE-T)		±300	±585	mV
V_{SRON2}	Receive Threshold Turn-On Voltage (Reduced Level)		±175	±300	mV
V_{SROFF}	Receive Threshold Turn-Off Voltage (Note 1)		±175	V_{SRON} − 100	mV
V_{DIFF}	Differential Mode Input Voltage Range (Note 1)	V_{CC} = 5.0V	−3.1	+3.1	V

Note 1: This parameter is guaranteed by design and is not tested.

Obsolete

15.0 Switching Characteristics AC Specs DP83902A **Note:** All Timing is Preliminary

Register Read (Latched Using ADS0)



TL/F/11157–33

Symbol	Parameter	Min	Max	Units
rss	Register Select Setup to ADS0 Low	10		ns
rsh	Register Select Hold from ADS0 Low	13		ns
aswi	Address Strobe Width In	15		ns
ackdv	Acknowledge Low to Data Valid		55	ns
rdz	Read Strobe to Data TRI-STATE (Note 3)	15	70	ns
rackl	Read Strobe to $\overline{ACK}$ Low (Notes 1, 2)		n*bcyc + 30	ns
rackh	Read Strobe to $\overline{ACK}$ High		30	ns
rsrsl	Register Select to Slave Read Low, Latched RS0–3	10		ns

Note 1: $\overline{ACK}$ is not generated until $\overline{CS}$ and $\overline{SRD}$ are low and the ST-NIC has synchronized to the register access. The ST-NIC will insert an integral number of Bus Clock cycles until it is synchronized. In Dual Bus systems additional cycles will be used for a local or remote DMA to complete. Wait states must be issued to the CPU until $\overline{ACK}$ is asserted low.

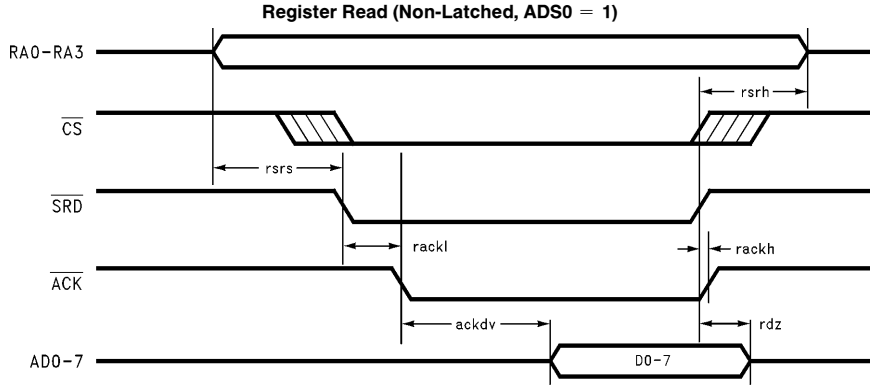
Note 2: $\overline{CS}$ may be asserted before or after $\overline{SRD}$. If $\overline{CS}$ is asserted after $\overline{SRD}$, rackl is referenced from falling edge of $\overline{CS}$. $\overline{CS}$ can be de-asserted concurrently with $\overline{SRD}$ or after $\overline{SRD}$ is de-asserted.

Note 3: These limits include the RC delay inherent in our test method. These signals typically turn off within 15 ns, enabling other devices to drive these lines with no contention.

Obsolete

15.0 Switching Characteristics AC Specs DP83902A **Note:** All Timing is Preliminary (Continued)

Register Read (Non-Latched, ADS0 = 1)



TL/F/11157–34

Symbol	Parameter	Min	Max	Units
rsrs	Register Select to Read Setup (Notes 1, 3)	10		ns
rsrh	Register Select Hold from Read	0		ns
ackdv	$\overline{ACK}$ Low to Valid Data		55	ns
rdz	Read Strobe to Data TRI-STATE (Note 2)	15	70	ns
rackl	Read Strobe to $\overline{ACK}$ Low (Note 3)		n*bcyc + 30	ns
rackh	Read Strobe to $\overline{ACK}$ High		30	ns

Note 1: rsrs includes flow-through time of latch.

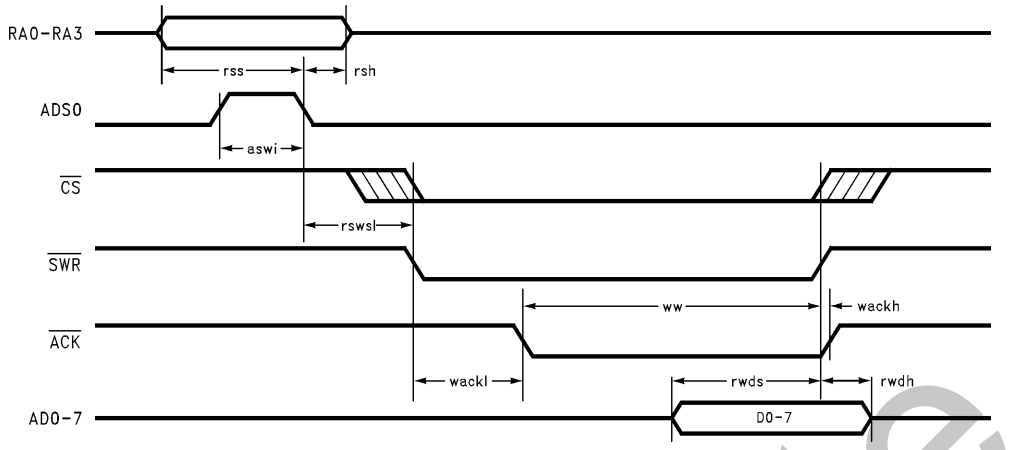
Note 2: These limits include the RC delay inherent in our test method. These signals typically turn off within 15 ns enabling other devices to drive these lines with no contention.

Note 3: $\overline{CS}$ may be asserted before of after RA0–3, and $\overline{SRD}$, since address decode begins when $\overline{ACK}$ is asserted. If $\overline{CS}$ is asserted after RA0–3, and $\overline{SRD}$, rackl is referenced from falling edge of $\overline{CS}$.

Obsolete

15.0 Switching Characteristics AC Specs DP83902A **Note:** All Timing is Preliminary (Continued)

Register Write (Latched Using ADS0)



TL/F/11157–35

Symbol	Parameter	Min	Max	Units
rss	Register Select Setup to ADS0 Low	10		ns
rsh	Register Select Hold from ADS0 Low	17		ns
aswi	Address Strobe Width In	15		ns
rwds	Register Write Data Setup	20		ns
rwdh	Register Write Data Hold	21		ns
ww	Write Strobe Width from $\overline{ACK}$	50		ns
wackh	Write Strobe High to $\overline{ACK}$ High		30	ns
wackl	Write Low to $\overline{ACK}$ Low (Notes 1, 2)		n*bcyc + 30	ns
rswsl	Register Select to Write Strobe Low	10		ns

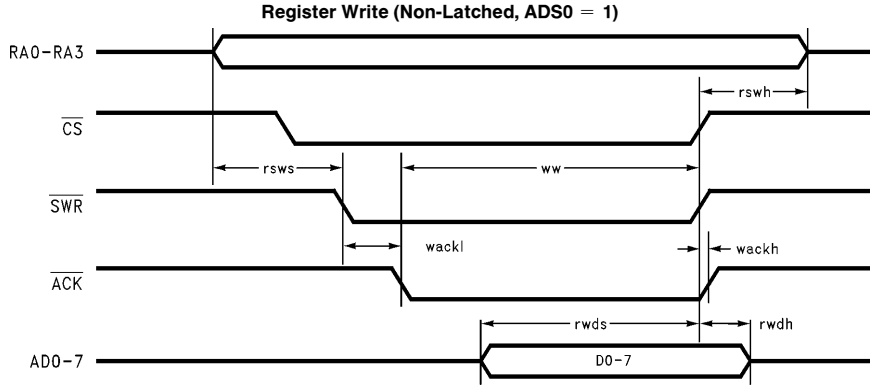
Note 1: $\overline{ACK}$ is not generated until $\overline{CS}$ and $\overline{SWR}$ are low and the ST-NIC has synchronized to the register access. In Dual Bus Systems additional cycles will be used for a local DMA or Remote DMA to complete.

Note 2: $\overline{CS}$ may be asserted before or after $\overline{SWR}$. If $\overline{CS}$ is asserted after $\overline{SWR}$, wackl is referenced from falling edge of $\overline{CS}$.

Obsolete

15.0 Switching Characteristics AC Specs DP83902A **Note:** All Timing is Preliminary (Continued)

Register Write (Non-Latched, ADS0 = 1)



TL/F/11157–36

Symbol	Parameter	Min	Max	Units
rsws	Register Select to Write Setup (Note 1)	15		ns
rswh	Register Select Hold from Write	0		ns
rwds	Register Write Data Setup	20		ns
rwdh	Register Write Data Hold	21		ns
wackl	Write Low to $\overline{ACK}$ Low (Note 2)		n*bcyc + 30	ns
wackh	Write High to $\overline{ACK}$ High		30	ns
ww	Write Width from $\overline{ACK}$	50		ns

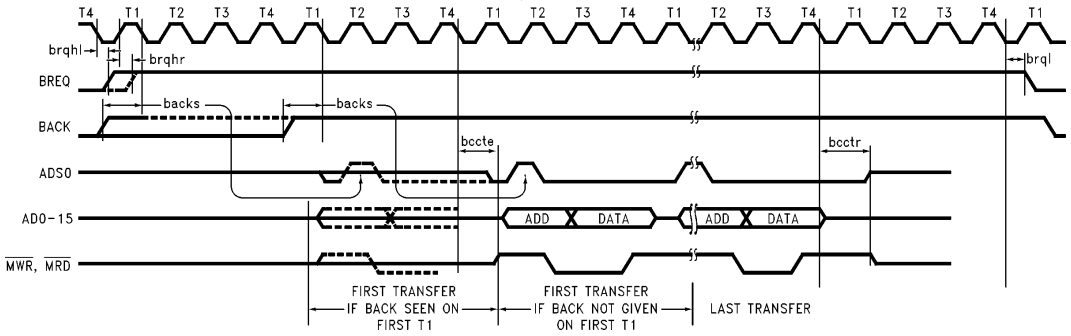
Note 1: Assumes ADS0 is high when RA0–3 changing.

Note 2: $\overline{ACK}$ is not generated until $\overline{CS}$ and $\overline{SWR}$ are low and the ST-NIC has synchronized to the register access. In Dual Bus systems additional cycles will be used for a local DMA or remote DMA to complete.

Obsolete

15.0 Switching Characteristics AC Specs DP83902A **Note:** All Timing is Preliminary (Continued)

DMA Control, Bus Arbitration



TL/F/11157–37

Symbol	Parameter	Min	Max	Units
brqhl	Bus Clock to Bus Request High for Local DMA		50	ns
brqhr	Bus Clock to Bus Request High for Remote DMA		45	ns
brql	Bus Request Low from Bus Clock		60	ns
backs	Acknowledge Setup to Bus Clock (Note 1)	2		ns
bccte	Bus Clock to Control Enable		60	ns
bcctr	Bus Clock to Control Release (Notes 2, 3)		70	ns

Note 1: BACK must be setup before T1 after BREQ is asserted. Missed setup will slip the beginning of the DMA by four bus clocks. The Bus Latency will influence the allowable FIFO threshold.

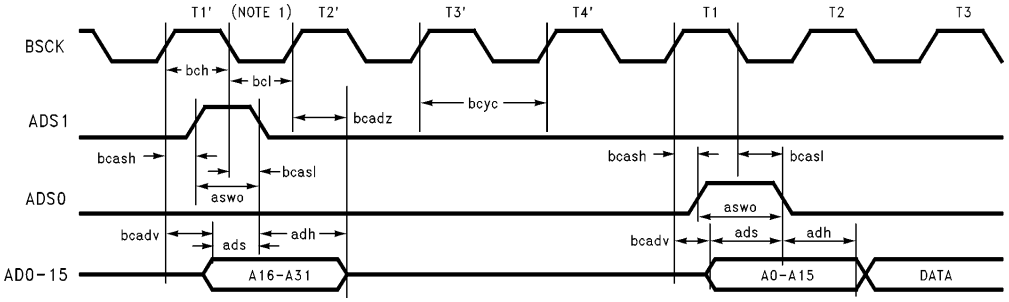
Note 2: During remote DMA transfers only, a single bus transfer is performed. During local DMA operations burst mode transfers are performed.

Note 3: These limits include the RC delay inherent in our test method. These signals typically turn off within 15 ns enabling other devices to drive these lines with no contention.

Obsolete

15.0 Switching Characteristics AC Specs DP83902A **Note:** All Timing is Preliminary (Continued)

DMA Address Generation



TL/F/11157–38

Symbol	Parameter	Min	Max	Units
bcyc	Bus Clock Cycle Time (Note 2)	50	125	ns
bch	Bus Clock High Time	20		ns
bcl	Bus Clock Low Time	20		ns
bcash	Bus Clock to Address Strobe High		34	ns
bcasl	Bus Clock to Address Strobe Low		44	ns
aswo	Address Strobe Width Out	bch		ns
bcadv	Bus Clock to Address Valid		45	ns
bcadz	Bus Clock to Address TRI-STATE (Note 3)	15	55	ns
ads	Address Setup to ADS0/1 Low	bch − 15		ns
adh	Address Hold from ADS0/1 Low	bcl − 5		ns

Note 1: Cycles T1′, T2′, T3′ and T4′ are only issued for the first transfer in a burst when 32-bit mode has been selected.

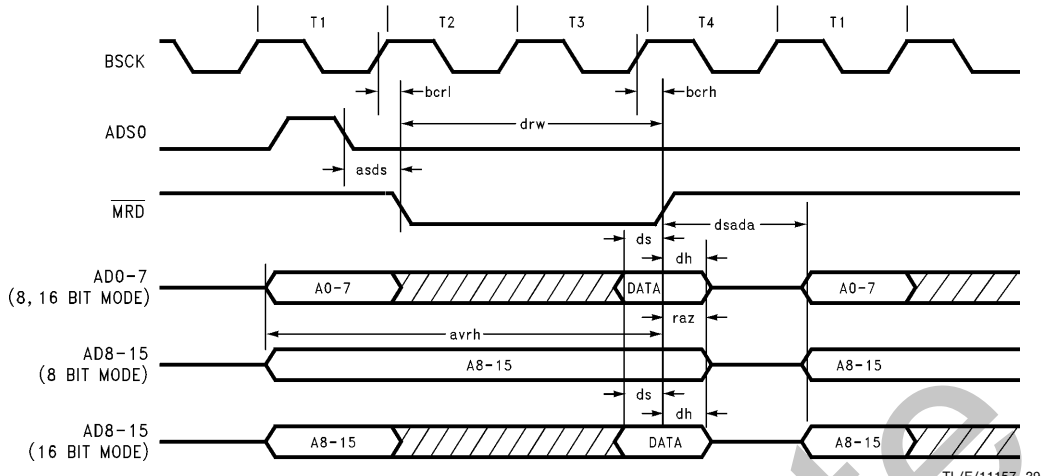
Note 2: The rate of bus clock must be high enough to support transfers to/from the FIFO at a rate greater than the serial network transfers from/to the FIFO.

Note 3: These limits include the RC delay inherent in our test method. These signals typically turn off within 15 ns, enabling other devices to drive these lines with no contention.

Obsolete

15.0 Switching Characteristics AC Specs DP83902A **Note:** All Timing is Preliminary (Continued)

DMA Memory Read



TL/F/11157–39

Symbol	Parameter	Min	Max	Units
bcrl	Bus Clock to Read Strobe Low		43	ns
bcrh	Bus Clock to Read Strobe High		40	ns
ds	Data Setup to Read Strobe High	22		ns
dh	Data Hold from Read Strobe High	0		ns
drw	DMA Read Strobe Width Out	2*bcyc − 15		ns
raz	Memory Read High to Address TRI-STATE (Notes 1, 2)		bch + 40	ns
asds	Address Strobe to Data Strobe		bcl + 10	ns
dsada	Data Strobe to Address Active	bcyc − 10		ns
avrh	Address Valid to Read Strobe High	3*bcyc − 18		ns

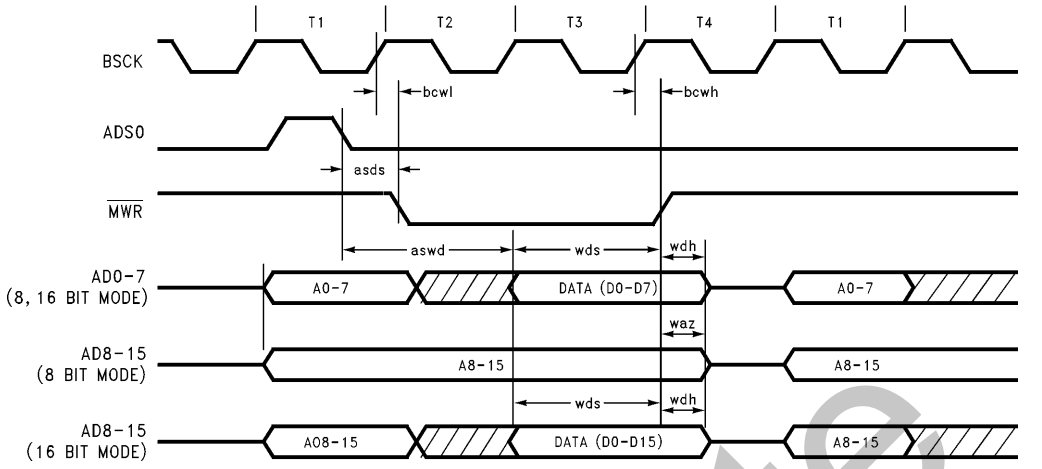
Note 1: During a burst A8–A15 are not TRI-STATE if byte wide transfers are selected. On the last transfer A8–A15 are TRI-STATE as shown above.

Note 2: These limits include the RC delay inherent in our test method. These signals typically turn off within bch + 15 ns, enabling other devices to drive these lines with no contention.

Obsolete

15.0 Switching Characteristics AC Specs DP83902A **Note:** All Timing is Preliminary (Continued)

DMA Memory Write



TL/F/11157–40

Symbol	Parameter	Min	Max	Units
bcwl	Bus Clock to Write Strobe Low		40	ns
bcwh	Bus Clock to Write Strobe High		40	ns
wds	Data Setup to $\overline{\text{MWR}}$ High	2*bcyc − 30		ns
wdh	Data Hold from $\overline{\text{MWR}}$ Low	bch + 7		ns
waz	Write Strobe to Address TRI-STATE (Notes 1, 2)		bch + 40	ns
asds	Address Strobe to Data Strobe		bcl + 10	ns
aswd	Address Strobe to Write Data Valid		bcl + 30	ns

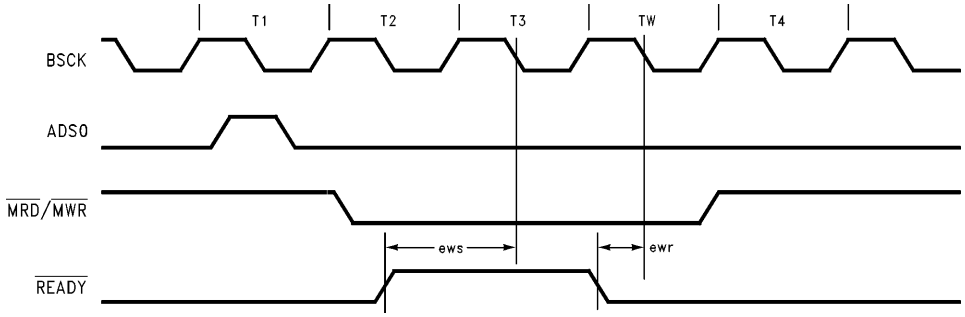
Note 1: When using byte mode transfers A8–A15 are only TRI-STATE on the last transfer, waz timing is only valid for last transfer in a burst.

Note 2: These limits include the RC delay inherent in our test method. These signals typically turn off within bch + 15 ns, enabling other devices to drive these lines with no contention.

Obsolete

15.0 Switching Characteristics AC Specs DP83902A **Note:** All Timing is Preliminary (Continued)

Wait State Insertion



TL/F/11157–41

Symbol	Parameter	Min	Max	Units
ews	External Wait Setup to T3 0Clock (Note 1)	10		ns
ewr	External Wait Release Time (Note 1)	15		ns

Note 1: The addition of wait states affects the count of deserialized bytes and is limited to a number of bus clock cycles depending on the bus clock and network rates. The allowable wait states are found in the table below. (Assumes 10 Mbit/sec data rate.)

BSCK (MHz)	Max # of Wait States	
	Byte Transfer	Word Transfer
8	0	1
10	0	1
12	1	2
14	1	2
16	1	3
18	2	3
20	2	4

Table assumes 10 MHz network clock.

The number of allowable wait states in byte mode can be calculated using:

$$\#W_{(\text{byte mode})} = \left(\frac{8\ tnw}{4.5\ tbsck} - 1\right)$$

#W = Number of Wait States
tnw = Network Clock Period
tbsck = BSCK Period

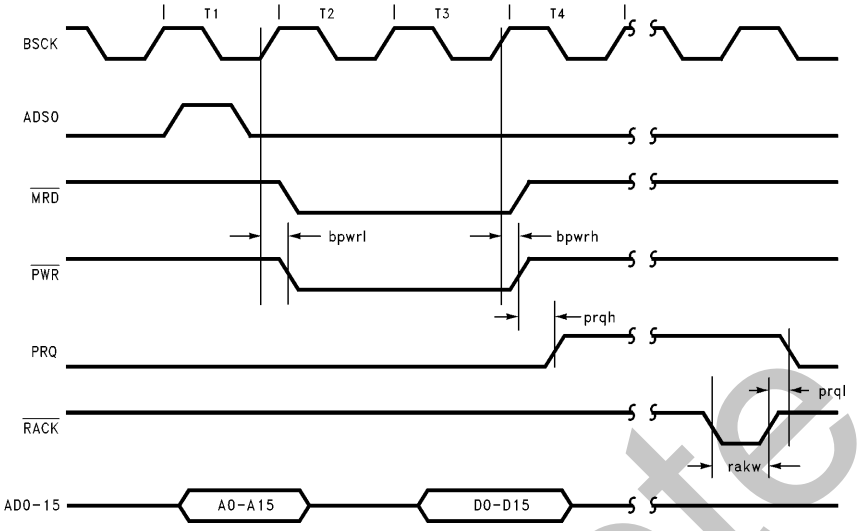
The number of allowable wait states in word mode can be calculated using:

$$\#W_{(\text{word mode})} = \left(\frac{5\ tnw}{2\ tbsck} - 1\right)$$

Obsolete

15.0 Switching Characteristics AC Specs DP83902A **Note:** All Timing is Preliminary (Continued)

Remote DMA (Read, Send Command)



TL/F/11157–42

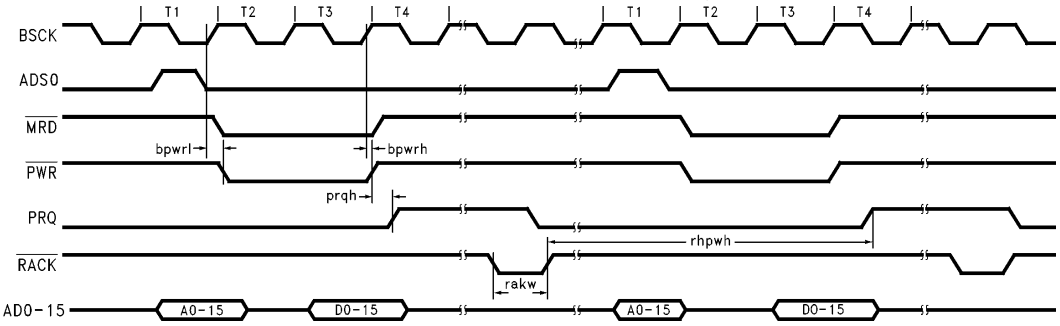
Symbol	Parameter	Min	Max	Units
bpwrl	Bus Clock to Port Write Low		43	ns
bpwrh	Bus Clock to Port Write High		40	ns
prqh	Port Write High to Port Request High (Note 1)		30	ns
prql	Port Request Low from Read Acknowledge High		60	ns
rakw	Remote Acknowledge Read Strobe Pulse Width	20		ns

Note 1: Start of next transfer is dependent on where $\overline{\text{RACK}}$ is generated relative to BSCK and whether a local DMA is pending.

Obsolete

15.0 Switching Characteristics AC Specs DP83902A **Note:** All Timing is Preliminary (Continued)

Remote DMA (Read, Send Command) Recovery Time



TL/F/11157–43

Symbol	Parameter	Min	Max	Units
bpwrl	Bus Clock to Port Write Low		43	ns
bpwrh	Bus Clock to Port Write High		40	ns
prqh	Port Write High to Port Request High (Note 1)		30	ns
prql	Port Request Low from Read Acknowledge High		60	ns
rakw	Remote Acknowledge Read Strobe Pulse Width	20		ns
rhpwh	Read Acknowledge High to Next Port Write Cycle (Notes 2, 3, 4)	11		BSCK

Note 1: Start of next transfer is dependent on where $\overline{\text{RACK}}$ is generated relative to BSCK and whether or not a local DMA is pending.

Note 2: This is not a measured value but guaranteed by design.

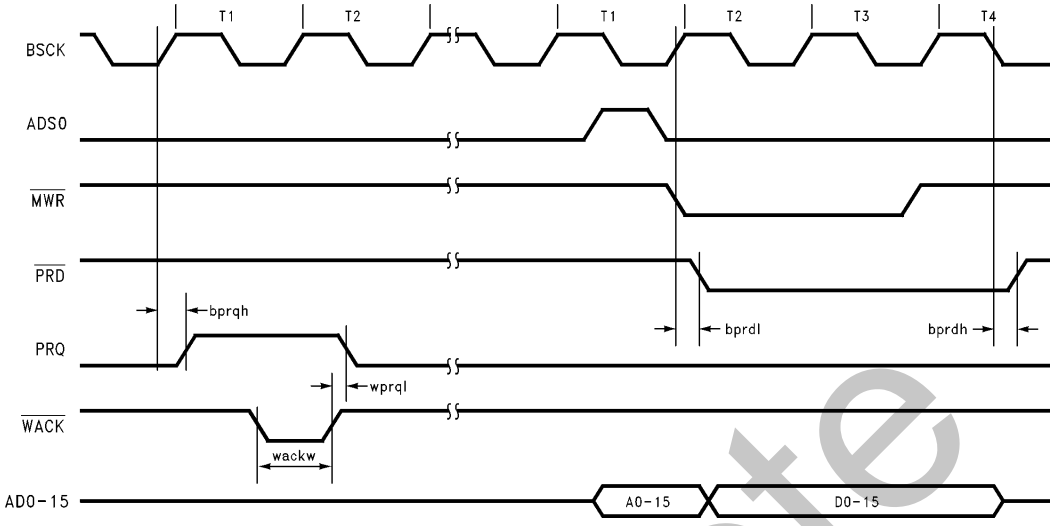
Note 3: $\overline{\text{RACK}}$ must be high for a minimum of 7 BSCK.

Note 4: Assumes no local DMA interleave, no $\overline{\text{CS}}$, and immediate BACK.

Obsolete

15.0 Switching Characteristics AC Specs DP83902A **Note:** All Timing is Preliminary (Continued)

Remote DMA (Write Cycle)



TL/F/11157–44

Symbol	Parameter	Min	Max	Units
bprqh	Bus Clock to Port Request High (Note 1)		42	ns
wprql	$\overline{\text{WACK}}$ to Port Request Low		52	ns
wackw	$\overline{\text{WACK}}$ Pulse Width	25		ns
bprdl	Bus Clock to Port Read Low (Note 2)		55	ns
bprdh	Bus Clock to Port Read High		40	ns

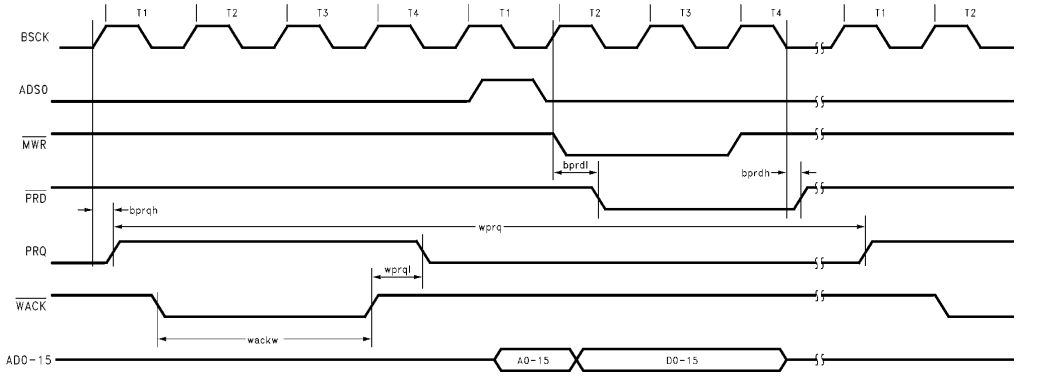
Note 1: The first port request is issued in response to the remote write command. It is subsequently issued on T1 clock cycles following completion of remote DMA cycles.

Note 2: The start of the remote DMA write following $\overline{\text{WACK}}$ is dependent on where $\overline{\text{WACK}}$ is issued relative to BSCK and whether a local DMA is pending.

Obsolete

15.0 Switching Characteristics AC Specs DP83902A **Note:** All Timing is Preliminary (Continued)

Remote DMA (Write Cycle) Recovery Time



TL/F/11157–45

Symbol	Parameter	Min	Max	Units
bprqh	Bus Clock to Port Request High (Note 1)		42	ns
wprql	$\overline{WACK}$ to Port Request Low		50	ns
wackw	$\overline{WACK}$ Pulse Width	25		ns
bprdl	Bus Clock to Port Read Low (Note 2)		55	ns
bprdh	Bus Clock to Port Read High		40	ns
wprq	Remote Write Port Request to Port Request Time (Notes 3, 4, 5)	12		BSCK

Note 1: The first port request is issued in response to the remote write command. It is subsequently issued on T1 clock cycles following completion of remote DMA cycles.

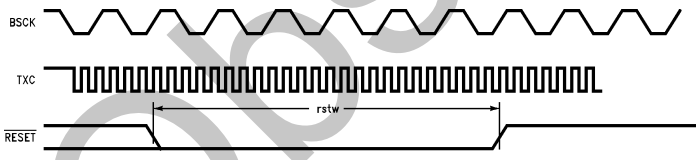
Note 2: The start of the remote DMA write following $\overline{WACK}$ is dependent on where $\overline{WACK}$ is issued relative to BSCK and whether a local DMA is pending.

Note 3: Assuming wackw $<$ 1 BSCK, and no local DMA interleave, no $\overline{CS}$, immediate $\overline{BACK}$, and $\overline{WACK}$ goes high before T4.

Note 4: $\overline{WACK}$ must be high for a minimum of 7 BSCK.

Note 5: This is not a measured value but guaranteed by design.

Reset Timing



TL/F/11157–64

Symbol	Parameter	Min	Max	Units
rstw	Reset Pulse Width (Note 1)	8		BSCK Cycles or TXC Cycles (Note 2)

Note 1: The RESET pulse requires that BSCK and TXC be stable. On power up, $\overline{RESET}$ should not be raised until BSCK and TXC have become stable. Several registers are affected by $\overline{RESET}$. Consult the register descriptions for details.

Note 2: The slower of BSCK or TXC clocks will determine the minimum time for the $\overline{RESET}$ signal to be low.

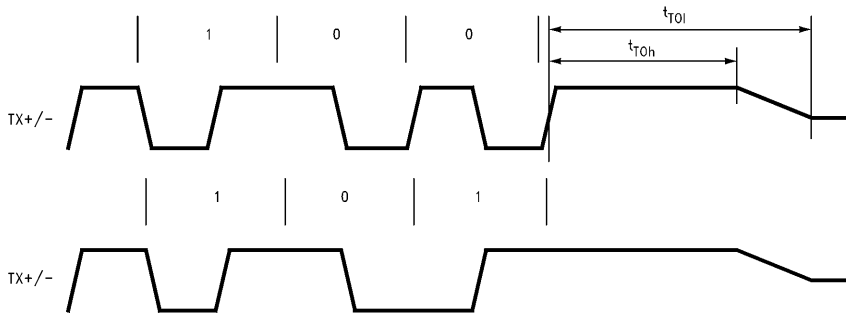
If BSCK $<$ TXC then $\overline{RESET}$ $=$ 8 $\times$ BSCK

If TXC $<$ BSCK then $\overline{RESET}$ $=$ 8 $\times$ TXC

Obsolete

15.0 Switching Characteristics AC Specs DP83902A **Note:** All Timing is Preliminary (Continued)

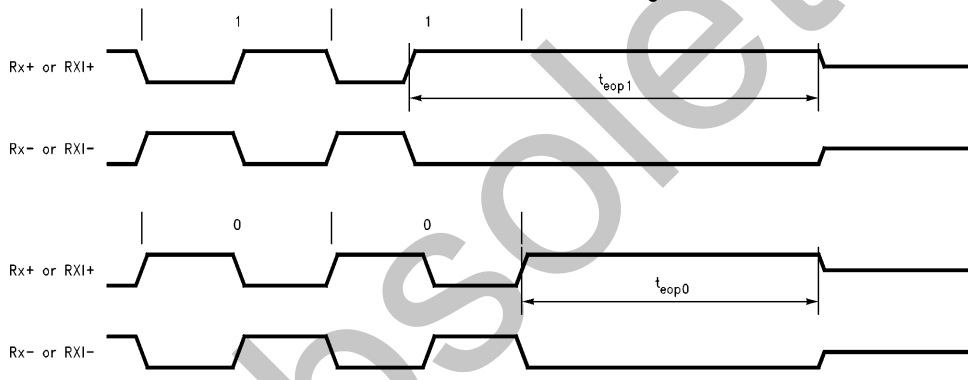
AUI Transmit Timing (End of Packet)



TL/F/11157–46

Symbol	Parameter	Min	Max	Units
t_{TOh}	Transmit Output High before Idle (Half Step)	200		ns
t_{TOI}	Transmit Output Idle Time (Half Step)		8000	ns

AUI/TPI Receive End of Packet Timing



TL/F/11157–47

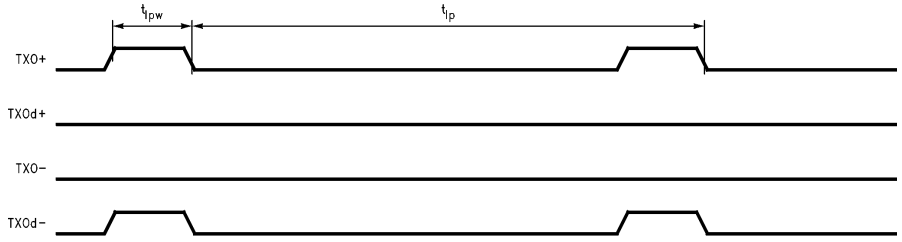
Symbol	Parameter	Min	Max	Units
teop1	Receive End of Packet Hold Time after Logic "1" (Note 1)	225		ns
teop0	Receive End of Packet Hold Time after Logic "0" (Note 1)	225		ns

Note 1: This parameter is guaranteed by design and is not tested.

Obsolete

15.0 Switching Characteristics AC Specs DP83902A **Note:** All Timing is Preliminary (Continued)

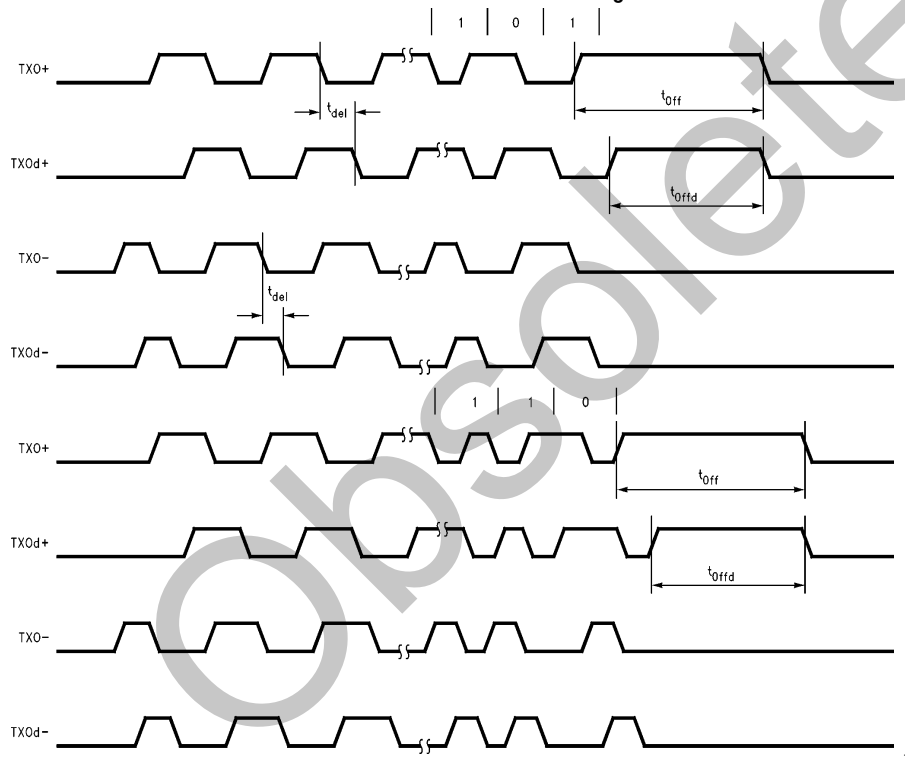
Link Pulse Timing



TL/F/11157–48

Symbol	Parameter	Min	Max	Units
tip	Time between Link Output Pulses	8	24	ms
tipw	Link Integrity Output Pulse Width	80	130	ns

TPI Transmit and End of Packet Timing



TL/F/11157–49

Symbol	Parameter	Min	Max	Units
tdel	Pre-Emphasis Output Delay (TXO ± to TXOd ±) (Note 1)	46	54	ns
toff	Transmit Hold Time at End of Packet (TXO ±) (Note 1)	250		ns
toffd	Transmit Hold Time at End of Packet (TXOd ±) (Note 1)	200		ns

Note 1: This parameter is guaranteed by design and is not tested.

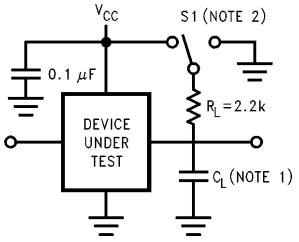
Obsolete

16.0 AC Timing Test Conditions

All specifications are valid only if the mandatory isolation is employed and all differential signals are taken to be at the AUI side of the pulse transformer.

Input Pulse Levels (TTL/CMOS)	GND to 3.0V
Input Rise and Fall Times (TTL/CMOS)	5 ns
Input and Output Reference Levels (TTL/CMOS)	1.3V
Input Pulse Levels (Diff.)	−350 mV to −1315 mV
Input and Output Reference Levels (Diff.)	50% Point of the Differential
TRI-STATE Reference Levels	Float (Δ V) ±0.5V

Output Load (See Figure Below)



TL/F/11157–50

Note 1: 50 pF, includes scope and jig capacitance.

Note 2: S1 = Open for timing tests for push pull outputs.

S1 = V_{CC} for V_{OL} test.

S1 = GND for V_{OH} test.

S1 = V_{CC} for High Impedance to active low and active low to High Impedance measurements.

S1 = GND for High Impedance to active high and active high to High Impedance measurements.

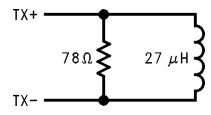
Pin Capacitance T_A = 25°C, f = 1 MHz

Symbol	Parameter	Typ	Units
C_{IN}	Input Capacitance	7	pF
C_{OUT}	Output Capacitance	7	pF

DERATING FACTOR

Output timing is measured with a purely capacitive load of 50 pF. The following correction factor can be used for other loads: $C_L \geq 50\ pF + 0.3\ ns/pF$.

AUI Transmit Test Load

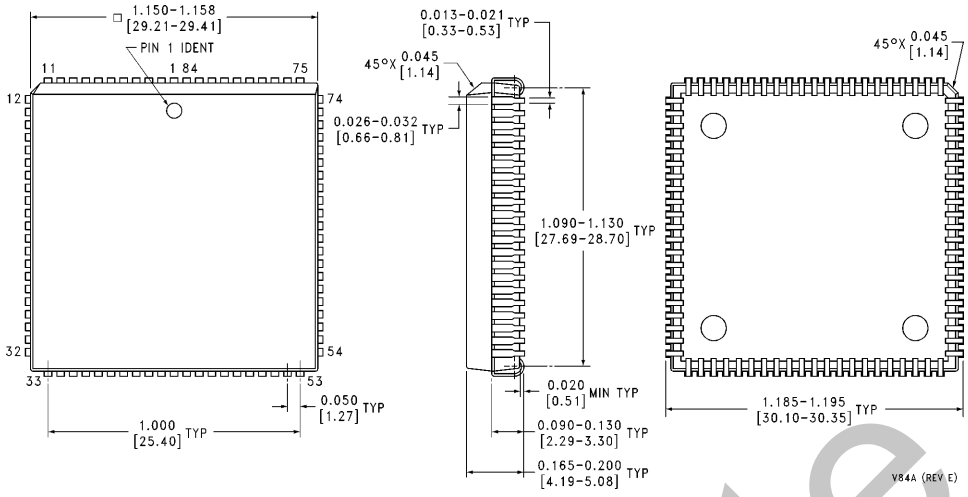


TL/F/11157–51

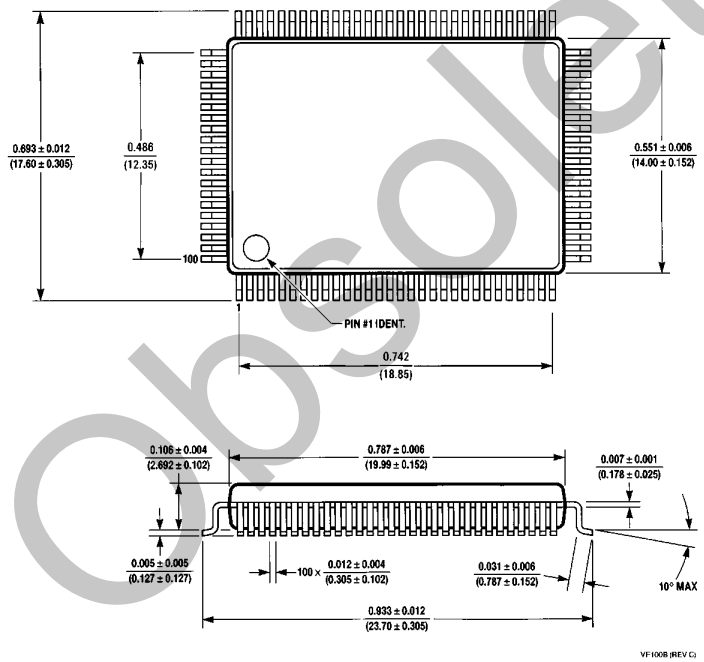
Note: In the above diagram, the TX+ and TX− signals are taken from the AUI side of the isolation (pulse transformer). The pulse transformer used for all testing is the Pulse Engineering PE64103.

Obsolete

17.0 Physical Dimensions inches (millimeters)



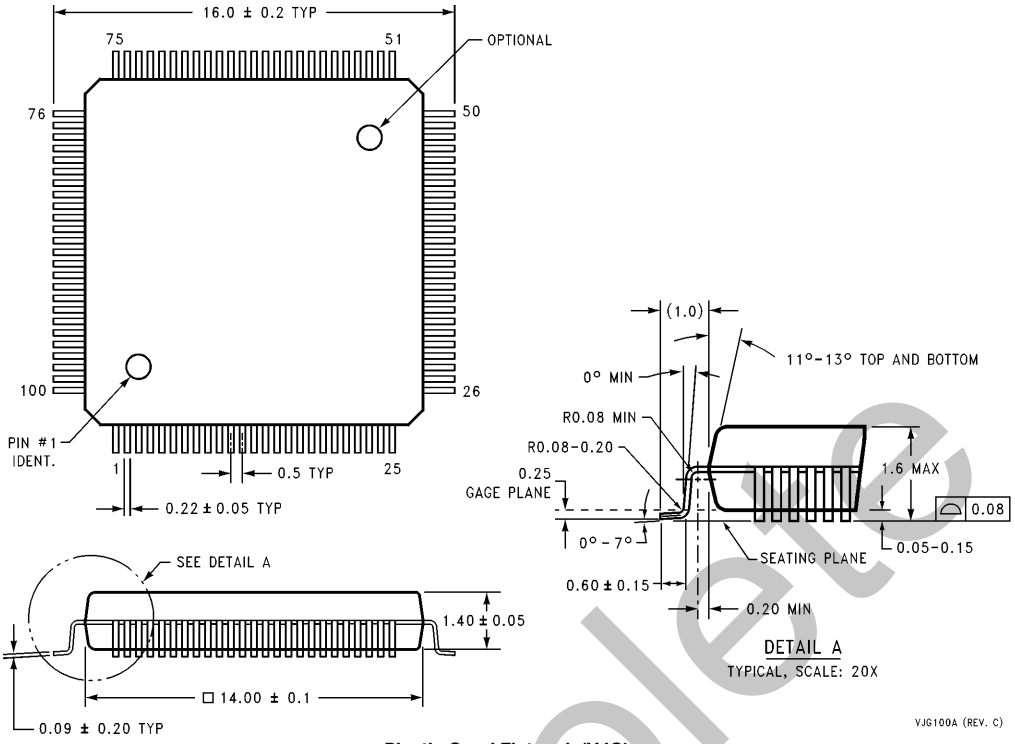
Plastic Chip Carrier (V)
Order Number DP83902AV
NS Package Number V84A



100 Pin Quad Flat Pack
Order Number DP83902AVF
NS Package Number VF100B

Obsolete

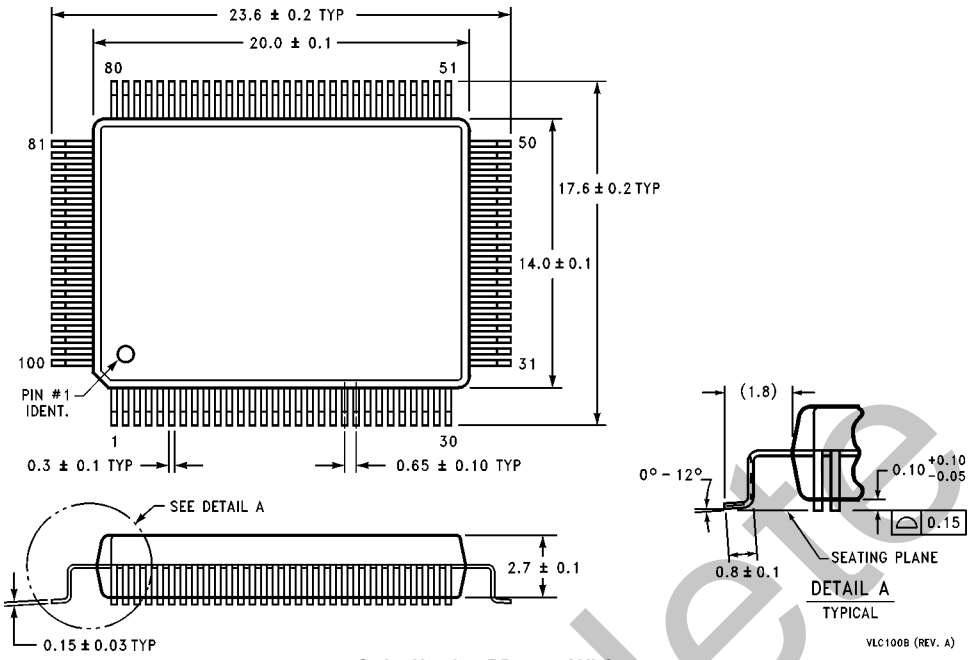
17.0 Physical Dimensions inches (millimeters) (Continued)



Plastic Quad Flatpack (VJG)
Order Number DP83902AVJG
NS Package Number VJG100A

Obsolete

17.0 Physical Dimensions inches (millimeters) (Continued)



Order Number DP83902AVLC
NS Package Number VLC100B

Obsolete

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